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I. PURPOSE

The purpose of this contract is to design and develop a silicon, ultra-high frequency power transistor capable of delivering 5 watts at 500 megacycles with minimums of 50 percent efficiency and 10db power gain. The device will be constructed in accordance with Signal Corps Technical Requirements No. SCL-7002/111 dated 23 August 1961. These requirements are listed below.

A. SPECIFICATIONS

MAXIMUM RATINGS AT 25°C

Parameter	Rating
BV_{CEO}	75 Vdc
BV_{EBO}	5 Vdc
LV_{CER}	60 Vdc at $R \geq 10\ \Omega$
P_c	12 watts at 25°C case temp.
I_c	1.0 Adc
T_j	200°C
T_{stg}	-65°C to 200°C

GROUP A INSPECTION

Examination or Test	Conditions	Symbol	Limits Min	Limits Max	Units
Collector Cut-off Current	V_{CE} = 75Vdc, I_b = 0	I_{CEO}	-	100	μAdc
Collector Cut-off Current	V_{CE} = 28Vdc, V_{EB} = 0	I_{CES}	-	1	μAdc

Examination or Test	Conditions	Symbol	Limits Min	Max	Units
Collector Cut-off Current	V_{CE} = 75V V_{EB} = 0	I_{CES}	-	100	μAdc
Sustaining Voltage	I_C = 50mAdc	LV_{CER}	60	-	Vdc
Emitter Cut-off Current	V_{EB} = 5Vdc I_C = 0	I_{EBO}	-	100	μAdc
Static Forward Current Transfer Ratio	V_{CE} = 28Vdc I_C = 357mAdc	h_{FE}	20	60	-
Base Spreading Resistance	V_{CE} = 28Vdc I_C = 357mAdc	rb'	-	10	ohms
Output Capacitance	V_{CB} = 28V I_E = 0	C_{ob}	-	5	μμf
Small Signal Short Circuit Forward Current Transfer Ratio	V_{CE} = 28Vdc I_C = 357ma f = 500 mc	h_{fe}	12	-	db
Saturation Voltage	I_C = 700mAdc I_B = 150mAdc	V_{CE}(sat)	-	0.5	Volts
Power Gain	V_{CE} = 28Vdc I_C = 357mAdc f = 500mc P_i = 0.5 watts T_C < 55°C	P.G.	10	-	db
Oscillator Output	V_{CE} = 28Vdc I_C = 357mAdc F = 500mc	P. O.	5	-	Watts

In addition to the above, a Group B inspection shall be performed, consisting of the following examinations and tests.

GROUP B INSPECTION

Examination or Test	Conditions	Symbol	Limits Min	Limits Max	Units
Subgroup 1					
Soldering	-	-	-	-	-
Temperature Cycling	-65°C to 200°C 5 cycles	-	-	-	-
Moisture Resistance	-	-	-	-	-
Subgroup 2					
Shock	Non-operating 500g	-	-	-	-
Constant Acceleration	10,000g	-	-	-	-
Vibration, Fatigue	Non-operating	-	-	-	-
Vibration, Variable Frequency	-	-	-	-	-
Subgroup 3					
Thermal Resistance	-	θ_{J-C}	-	14.6	°C/W
Subgroup 4					
Storage Life	T = 200°C 1000 hours	-	-	-	-
Subgroups 1, 2 and 4 Test End Points					
Collector Cut-off Current	V_{CE} = 75Vdc I_B = 0	I_{CEO}	-	200	μAdc
Collector Cut-off Current	V_{CE} = 28Vdc V_{EB} = 0	I_{CES}	-	2	μAdc
Emitter Cutoff Current	V_{EB} = 5Vdc I_C = 0	I_{EBO}	-	200	μAdc

Examination or Test	Conditions	Symbol	Limits Min	Limits Max	Units
Static Forward Current Transfer Ratio	V_{CE} = 28Vdc I_C = 357mAdc	h_{FE}	18	-	-

B. CASE DESIGN AND CONSTRUCTION

The case shall be of the double ended stud type incorporating means for readily mounting the transistor. It shall also be electrically insulated from the collector, emitter and base.

II. ABSTRACT

An improved ultrahigh frequency transistor structure, called the overlay structure, has been designed which results in high emitter periphery to emitter area and emitter periphery to base area ratios. This structure incorporates many small individual sites to make up the necessary emitter periphery rather than a few continuous stripes as in the interdigitated structure.

Difficulties associated with the fabrication of this device resulted in the design of a diffused overlay structure which retains the advantages of the original device but reduces fabrication problems.

Experimental studies associated with the development of this device have resulted in significant state-of-the-art advances in the techniques of photomask fabrication, photolithography and diffusion.

Two hundred final transistors were submitted to the Contracting Agency. Power gain measurements of these devices, using a 500 megacycle Class C amplifier employing tuned lines, resulted in approximately 3.4 to 5.4 watts output. The median device had a power gain of 6.0 db at 4.0 watt output power.

III. PUBLICATIONS, REPORTS AND CONFERENCES

Since the last report period, a conference was held on 29 August 1963, at the United States Army Signal Research and Development Laboratories, Fort Monmouth, New Jersey between Mr. K. Fisher of the Signal Corps and representatives of Radio Corporation of America. The conference discussion included the progress on the modified overlay transistor and high frequency evaluation of the devices.

On 1 November 1963, a paper titled "A 5 W 500mc Transistor" was presented by Mr. D. R. Carley of the Radio Corporation of America at the PGED conference of the IEEE at Washington, D. C.

IV. FACTUAL DATA

A. DEVICE DESIGN

1. Introduction

During the past several years, Industrial and Military demands for more stringent transistor performance led to the development of devices of increased complexity.

Early work at RCA on high frequency, medium power transistors resulted in the development of the relatively simple stripe geometry, such as the 2N1493 and TA1938 (Figure 1), which has one emitter stripe and two adjacent base stripes. As transistor performance requirements for both output power and operating frequency were increased, new units were modified to the interdigitated (comb) structure with interleaved base and emitter fingers (Figure 2). Devices such as the RCA 2N2876 and TA2400 utilize this structure. In these comb type units, the emitter-base junction periphery is greatly increased allowing the transistor to operate at higher current levels and, hence, to deliver more output power.

As the frequency requirements of transistors extended into the upper VHF range, shunting capacitances inherent to the geometry of devices became increasingly important. Reductions in size and the tightening of tolerances of devices were necessary. This reduction in size to facilitate higher operating frequencies is not compatible with increases in emitter junction periphery necessary to increase

FIGURE 1 RELATIVELY SIMPLE STRIPE GEOMETRY DEVICE WITH BONDED LEADS

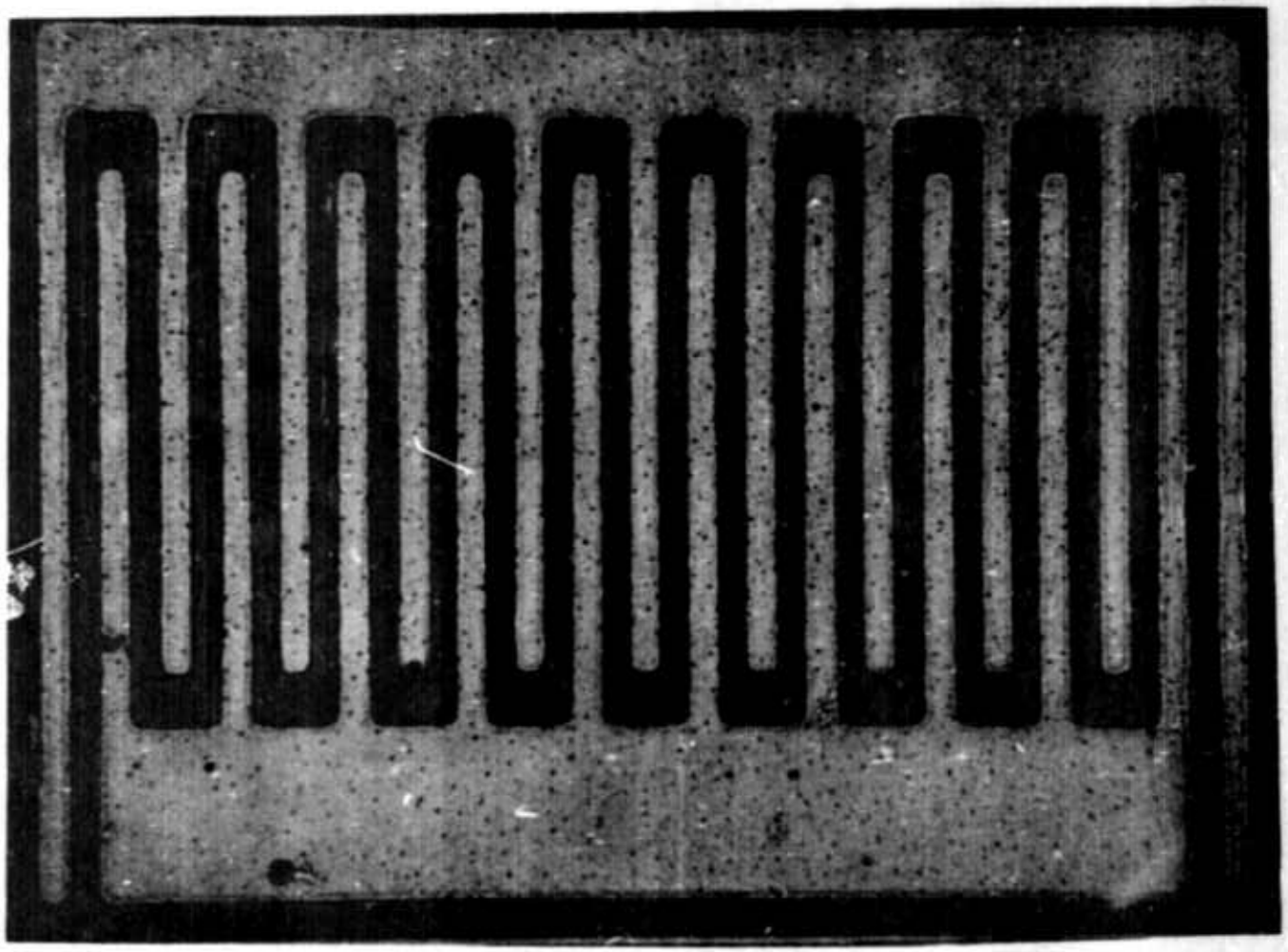


FIGURE 2 INTERDIGITATED (COMB) STRUCTURE WITH INTERLEAVED BASE AND EMITTER FINGERS

power output requirements.

Attempts to design high power transistors, operable in the UHF range, made it apparent that substantial improvements in fabrication techniques were necessary to meet both present day and future design requirements. Improved technology which would allow extremely accurate control of both diffusion and photolithic processes were needed. Preferably, these techniques should be utilized on an improved structure, which in itself, would afford design advantages not obtainable with a comb type structure.

2. Design Considerations

In the design of high power, high frequency transistors, the approximate structure of the device is determined by the specified static and dynamic operating characteristics. Thermal resistance, junction breakdown voltages, current gain, and high frequency considerations each dictate an optimum design. Because of the incompatibility of many of these "optimum designs" and with state-of-the-art fabrication techniques presently employed, the final design for these devices must be one which achieves the best compromise of these optimal designs.

The various parameters and their effect on the final design are discussed below.

a. Thermal Resistance

Power dissipation requirements control, to a large extent, the necessary active collector area. The active collector area

will be defined as that portion of the area within the collector base junction at the device surface.

Heat transfer calculations are subject to considerable uncertainty particularly under actual operating conditions and consequently, the required area is derived from empirical data. The calculations listed below use a theoretical approach and a comparison between the empirical and theoretical results are shown.

The heat generated from power dissipated in the device during operation must flow from the emitter through the silicon pellet and subsequent materials to the package ambient. This heat transfer must be high enough so that the temperature at the emitter base junction does not exceed 200°C during specified maximum power dissipation.

The thermal resistance of a device is defined as:

$$TR = \frac{T_J - T_C}{P} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where:

TR = thermal resistance in °C/Watt

T_J = junction temperature in °C

T_C = case temperature in °C

P = power dissipation in watts.

The design specifications require this device to be capable of 12 watts dissipation at a case temperature of 25°C. This

results in a maximum thermal resistance of 14.6°C/watt.

Measurements on earlier devices having an active collector area of 1532 square mils, mounted in the 7/16" double ended stud, isolated collector packages used on this program gave a thermal resistance of 4°C/watt. Calculations show that the case and the pellet each have a 2°C/watt thermal resistance. Subtracting the case component from the specified thermal resistance results in a maximum allowable pellet thermal resistance of 12.6°C/watt. Assuming an inverse linear relation between the active collector area and pellet thermal resistance, a minimum area of approximately 250 square mils is required. To allow for deviations from the linear assumption, a safety margin of 50 percent is employed fixing the active collector area and hence, base area at approximately 375 square mils in this device. Calculations using the relationship:

$$TR_2 = \frac{TR_1 A_1}{A_2} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

result in an expected pellet thermal resistance of 8.14°C/watt and a thermal resistance of 10.14°C/watt for the packaged device.

Thermal resistance may also be expressed as:

$$TR = \frac{t}{K A} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

where:

TR = thermal resistance in °C/watt

t = thickness of heat conducting medium

A = the cross sectional area of the conducting medium normal to the heat flow

K = heat conductivity in $\frac{\text{watts}}{\text{inch}^2\text{(area)}\ ^\circ\text{C/inch (length)}}$.

Figure 3a shows the pellet and stud geometry used in transistor construction. In this device, the entire emitter periphery is contained within an area having a length and width of 17.3 and 15.9 mils, respectively, near the pellet surface.

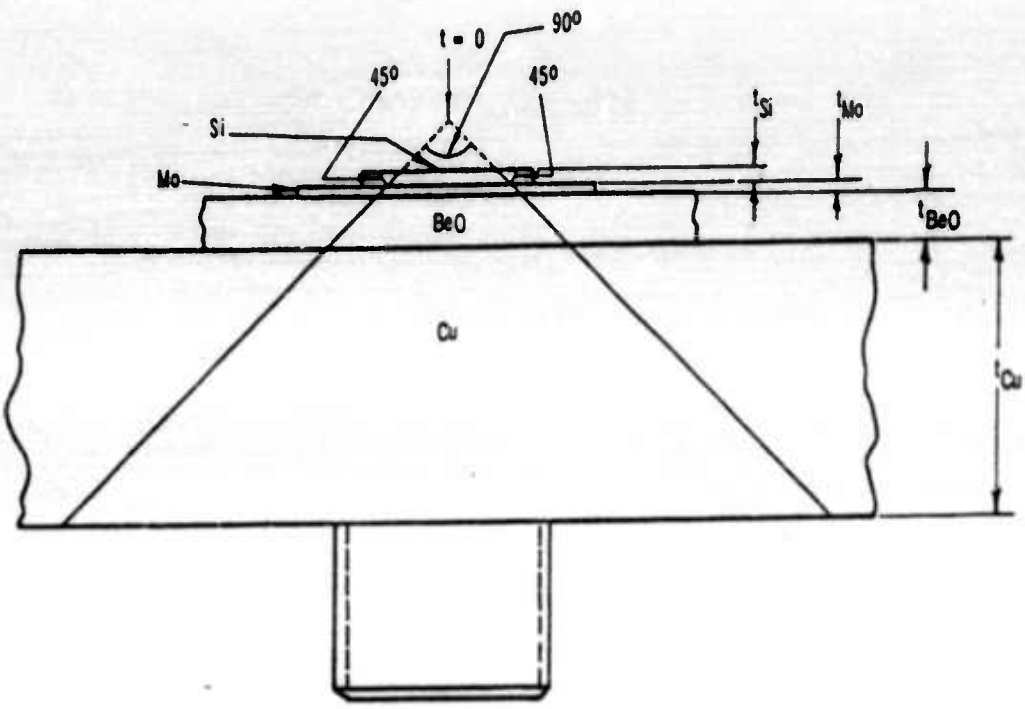
In the following calculations, a 45° boundary of heat transfer is assumed and discontinuities of heat flow at the interfaces are neglected. A solid angle heat flow is assumed.

Figure 3b shows a top view of the area of heat generation and the effective heat conducting areas of the various materials. The interfaces of these materials are shown at their distance from the zero origin.

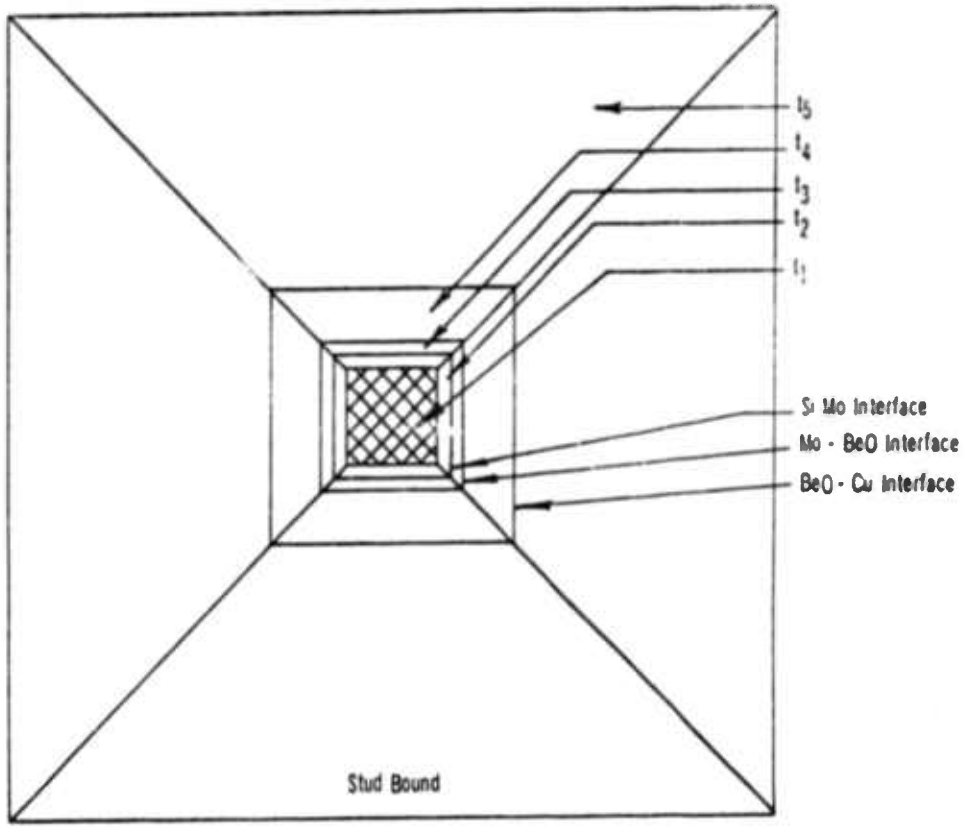
Referring to Figure 3a and 3b, the area of heat generation approximates a square having an average side length, s, of 16.6×10^{-3} inches. Since a 45° angle of heat conduction is assumed, then:

$$s = 2t$$

where: t is the distance from the origin of the system



a. Pellet and Stud Geometry Used in Transistor Construction



b. Top View - Heat Generation and Effective Heat Conducting Areas

TL3766

FIGURE 3 PELLET AND STUD GEOMETRY USED IN TRANSISTOR CONSTRUCTION AND TOP VIEW OF HEAT GENERATION AND EFFECTIVE HEAT CONDUCTING AREAS FOR VARIOUS MATERIALS

and $A = s^2 = 4t^2$.

Using Equation (3),

$$TR = \frac{t}{K A}$$

$$\text{and } TR = \int_{t_1}^{t_2} \frac{dt}{KA} = \frac{1}{K} \int_{t_1}^{t_2} \frac{dt}{4t^2} = -\frac{1}{4K} \left[\frac{1}{t} \right]_{t_1}^{t_2}$$

$$TR = -\frac{1}{4K} \left[\frac{1}{t_2} - \frac{1}{t_1} \right] = \frac{1}{4K} \left[\frac{t_2 - t_1}{t_2\, t_1} \right] = \frac{1}{4K} \left[\frac{t}{t_2\, t_1} \right] \quad .(4)$$

where t is the thickness of the particular conducting material. In the silicon pellet, $t_1 = \frac{s}{2} = 8.3 \times 10^{-3}$ inches and $t_2 = t_1 + 6 \times 10^{-3} = 14.3 \times 10^{-3}$ inches.

Therefore:

$$TR_{silicon} = \frac{1}{4(2.17)} \left[\frac{6 \times 10^{-3}}{(14.3)(8.3) \times 10^{-6}} \right]$$

$$= 5.83°C/watt \quad \ldots\ldots\ldots\ldots\ldots\ldots .(5)$$

Table I shows the coefficient of heat conductivity, the boundary thicknesses (t_1 and t_2), the material thickness (t) and the theoretical thermal resistance based on the above equations. The theoretical thermal resistance of the mounted pellet is the sum of the component resistances or 8.71°C/watt.

A comparison of the theoretical and empirical results shows a deviation of approximately 15 percent; however, both approaches indicate that an active collector area of 375 square mils is adequate.

TABLE I
THEORETICAL THERMAL RESISTANCE ON MATERIALS USED

Material	Coefficient of Thermal Conductivity $\frac{\text{Watts}}{^\circ\text{C inch}}$	Boundary Thickness t_2 inches x 10^{-3}	Boundary Thickness t_1 inches x 10^{-3}	Material Thickness t	Thermal Resistance TR-°C/Watt
Silicon	2.17	14.3	8.3	6	5.83
Molybdenum	3.76	19.3	14.3	5	1.20
Beryllium Oxide	5.65	41.3	19.3	22	1.22
Copper	9.8	166.3	41.3	125	0.46

b. Collector Base Breakdown Voltage

The choice of starting material resistivity is dependent on the required breakdown voltage, emitter to collector transit time, high frequency current gain and the required output capacitance. The optimum starting material is the lowest resistivity material which will support the required breakdown voltage.

The application of a reverse bias to a junction results in a depleting of majority carriers on both sides of the junction. The penetration of this depletion region is a function of the diffusion profile in the vicinity of the junction and the applied voltage. Under reverse bias conditions, charge neutrality must exist, that is, the net charge enclosed within the depletion region on the N and P sides of the junction must be zero.

The base width (W) and the width of the intrinsic region (the

original starting material between the base diffusion and the contact diffusion or low resistivity layer) may be determined by using the graphs developed by H. Lawrence and R. M. Warner, Jr.[1] and assuming a base surface concentration, junction depth and Gaussian impurity distribution. These curves predict total depletion layer thickness, the fraction of depletion thickness on each side of the junction, junction capacitance and peak electric field as a function of voltage for various junction depths and impurity concentrations.

To support 80 volts in 6 ohm-cm material, the base width must be 6.6×10^{-5} cm or about 0.026 mils because of the depletion region spread. Similarly, the intrinsic region width should be a minimum of 1.13×10^{-3} cm or 0.45 mils because of the spread into the collector body. (The base width and intrinsic region width should be greater to allow for any irregularity in the diffusion.)

Using 3 ohm-cm material, a base width of 5.4×10^{-5} cm (0.0214 mils) and an intrinsic region of 7.96×10^{-4} cm (0.313 mils) is necessary to support 80 volts.

The lower resistivity material can support the required breakdown voltage in a thinner depletion region. As will be discussed in later sections, it further results in a shorter emitter to collector transit time and an improved frequency

response at high current levels.

c. Collector Capacitance

The collector transition layer extends into both the base and collector body. Because of the difference in impurity gradient in the vicinity of the junction, only a small portion extends into the base. As previously discussed, the width of the depletion region (x_m) is an increasing function of voltage.

The collector capacitance can be characterized by the expression:

$$C_c = \frac{\epsilon_o \epsilon}{x_m} A_c \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

where:

ϵ_o = dielectric constant of free space

C_c = collector capacitance

ϵ = dielectric constant of the material

x_m = depletion layer width for a given voltage

A_c = active collector area.

Using 3 ohm-cm material and an active collector area of approximately 375 square mils, calculations indicate a collector capacitance of 4.9 $\mu\mu f$ at 30 volts. As can be seen, this value is very close to the specified maximum of 5$\mu\mu f$.

d. Collector Emitter Breakdown Voltage

The open base collector to emitter voltage (BV_{CEO}) relationship

for an NPN transistor can be expressed by an equation from Miller and Ebers:[2]

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{1 + h_{FE}}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (7)$$

The empirically derived avalanche multiplication exponent, n, has a typical value of 4 for silicon. The specifications of 75 Volt BV_{CEO} and a minimum h_{FE} of 20 results in a required avalanche breakdown of 160 volts. Graphical determination of avalanche breakdown from curves developed by D. P. Kennedy and R. R. O'Brien[3] predict a BV_{CBO} of 250 volts using 3 ohm-cm material. This value of avalanche represents the bulk breakdown in the silicon underneath the collector-base junction. In planar devices, the bulk avalanche breakdown is masked by surface breakdown phenomena which occur at much lower voltages than the bulk breakdown. Consequently, the limiting collector-base breakdown field is at the surface and not in the base at 80 volts. This field strength is not high enough to cause avalanching and lower BV_{CEO}, that is, BV_{CEO} is only slightly less than the measured surface limited BV_{CBO}.

e. Triple Diffused Structure

The triple diffused structure has been employed in the fabrication of this device to allow accurate control of the intrinsic region.

The diffusion profile is shown in Figure 4 and can be arrived at

by assuming an infinite source of impurity material necessary to provide a constant surface concentration, thus, producing an erfc impurity distribution. The formation of the collector base junction in the N- type intrinsic starting material can be expressed as:

$$C(x) = C_o \operatorname{erfc} \frac{x}{2\sqrt{Dt}} \quad \ldots\ldots\ldots\ldots (8)$$

where:

$C(x)$ = diffusant concentration at any point

C_o = surface concentration

x = depth from the surface

D = temperature dependent diffusion coefficient

t = diffusion time.

It is assumed that D, the diffusion coefficient of the diffusant, is a function only of temperature and not the diffusant atom concentration.

In the formation of the collector base junction, Equation(8) is used substituting the appropriate values for diffusing P-type diffusant into an N type intrinsic crystal.

In forming the emitter base junction, the N-type diffusant is going into a region with an erfc distribution on a previously diffused silicon surface. This can be expressed as:

$$C(x) = C_1 \operatorname{erfc} \frac{x}{2\sqrt{D_1 t_1}} - C_2 \operatorname{erfc} \frac{x}{2\sqrt{D_2 t_2}} + C_4 \quad \ldots (9)$$

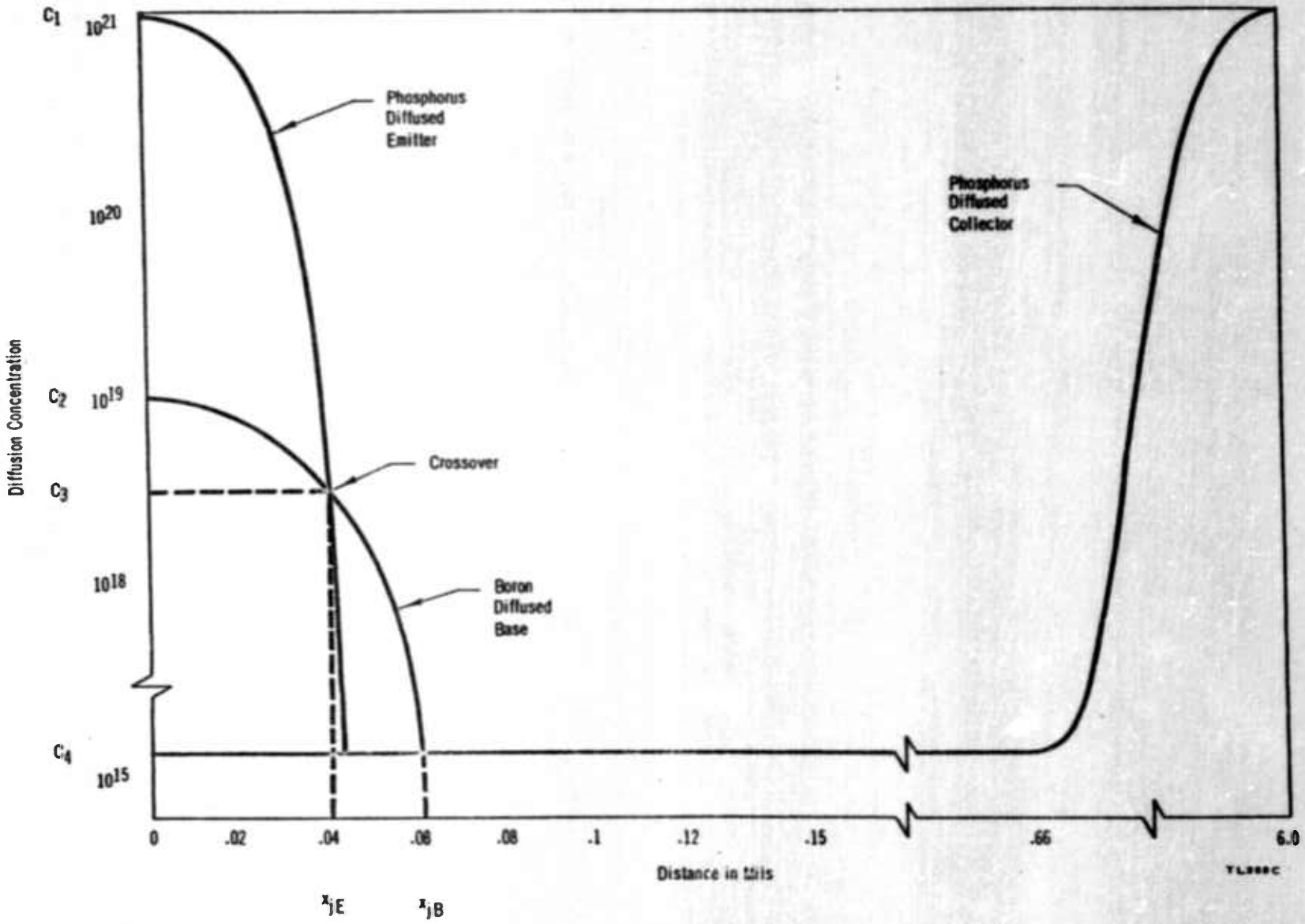


FIGURE 4 TA2307 DIFFUSION PROFILE

where:

C_1 = phosphorus surface concentration

D_1 = phosphorus diffusion coefficient

t_1 = phosphorus diffusion time

C_2 = boron surface concentration

D_2 = boron diffusion coefficient

t_2 = total diffusion time

C_3 = crossover concentration of the emitter junction

C_4 = N-type dopant concentration of the intrinsic material

C(x)=net N-type diffusant concentration at any point in the NPI portion of the transistor structure.

f. Emitter to Base Breakdown - V_{EBO}

The value of BV_{EBO} can be determined by employing the diffusion equation to obtain the emitter junction depth from:

$$C_3 = C_1 \operatorname{erfc} \frac{x_e}{L_1} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (10)$$

where:

C_1 = surface diffusant concentration

x_e = emitter junction depth

L_1 = diffusion length of the phosphorus emitter diffusion

C_3 = crossover concentration of the emitter junction.

The emitter diffusion length is used in Equation (11)[4]. ρ is the equivalent resistivity as calculated from the base surface concentration.

$$V_{EB} = 1500 \ (L_E \rho)^{0.364} \quad \ldots\ldots\ldots\ldots\ldots\ldots (11)$$

Curves developed by Kennedy and O'Brien[3] can also be used to approximate the emitter-base breakdown voltage. The emitter-base junction breaks down at the surface-boundary of the junction because the impurity gradient is at a maximum there(see Figure 3).

g. Current Gain and Emitter Periphery

In the design of high power transistors, serious consideration must be given to the relationship between current gain at high current and emitter junction periphery.

All transistors show a reduction of current gain with increasing current after reaching a maximum value. Initially, fields build up with additional carrier injection reducing the effect of surface recombination and thus, improving current gain.[5] As carrier injection continues to increase, emitter efficiency decreases due to a greater carrier concentration in the base region.

Investigations by Fletcher and others have shown that at high current densities a transverse voltage is developed in the base region causing carrier injection to be confined primarily to the edges of the emitter [2,6,7]. When considering Fletcher's theory, it is found that injection originates

from the emitter edge - a small percent of the total emitter area. This indicates that if devices are to be operated at high currents, with the desired current gain, large emitter peripheral length must be obtained in order to minimize the current density.

Empirical results show the maximum current gain occurs at an injection ratio of approximately 1.5 milliamperes per mil of junction length and are operable with good gain characteristic up to 4ma/mil. On the basis of the 357 milliampere average operating current, a peak current of approximately 1.1 amperes can be predicted in Class C operation. This value indicates a need for approximately 300 mils of emitter periphery to insure high values of current gain over the range of operating current.

b. Frequency Considerations

In order to obtain the required power gain of 10db at 500 megacycles, a gain-band value of merit (K) of approximately 1.6 KMC is necessary. This value is determined by assuming a 6db per octave power gain reduction with increasing frequency. The figure of merit, K, is expressed as:

$$K = (PG)^{1/2} F = \frac{1}{4\pi} \sqrt{\frac{1}{r_{bb'} C_c \tau_{ec}}} \quad \ldots\ldots (12)$$

where:

PG = power gain of the device

F = frequency of operation

$r_{bb'}$ = base resistance

C_c = collector capacitance

τ_{ec} = total emitter to collector transit time.

The value of the collector capacitance will be very close to the five picofarad upper limit of the specification and the value of the base resistance will be approximately 2 ohms, thus giving an $r_{bb'} C_c$ product of 10×10^{-10} seconds.

To achieve the specified power gain of 10 db at a frequency of 500 megacycles, a maximum total transit time of 2.5×10^{-10} seconds will be required. The current gain may also be used to determine the total transit time by using the following relationship:

$$h_{fe} = \frac{1}{2\pi f \tau_{ec}} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (13)$$

where:

h_{fe} = small signal short circuit forward current transfer ratio

f = frequency of operation

τ_{ec} = defined as above.

To achieve the specified current gain of 12db, an emitter to collector transit time of 8×10^{-11} seconds is necessary which is shorter than the value calculated from Equation (13). It must be realized that these equations (12,13) are developed from simplified equivalent circuits operating under low level, Class A amplifier conditions. However, they are useful approximations and the best calculations available. The emitter to collector delay time (τ_{ec}) is comprised of four terms: 1) the emitter transition capacitance charging

time (τ_e); the base layer transit time(τ_b); the collector depletion region transit time (τ_m); and the collector capacitance-collector series resistance charging time(τ_x). Of these terms, the collector capacitance-collector series resistance charging time can be neglected because the collector series resistance is very small making the value of this term approximately 10^{-12} seconds.

The value of emitter charging time(τ_e) can be related to other device parameters as follows:

$$\tau_e = \frac{kT}{qI_e} C_{ea} \quad \ldots\ldots\ldots\ldots\ldots\ldots (14)$$

where:

τ_e = emitter delay or transit time

k = Boltzmans Constant

T = temperature in degrees Kelvin

q = electron charge

I_e = emitter current

C_{ea} = emitter transition layer capacitance.

The emitter transition layer capacitance can be calculated as follows:

$$C_{ea} = A_e \left[\frac{q \epsilon \epsilon_o N_A}{2(V + V_1)} \right]^{1/2} \approx 28 \text{ picofarads} \quad \ldots (15)$$

where:

A_e = total emitter junction area

ϵ_o = dielectric constant of free space

ϵ = dielectric constant of silicon

N_A = acceptor density at the junction

$V+V_1$ = applied plus built in potential

q = electron charge.

The base transit time can be calculated from:

$$\tau_b = \frac{W^2}{2D_e} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (16)$$

where:

τ_b = base transit time

W = base width

D_e = diffusion constant for electrons in the base, approximately 23cm^2/sec.

The base width(W) varies with the collector potential because of the depletion region spread and must be sufficiently large to contain the depletion region (i.e., prevent punch-through). As previously discussed, the extent of the depletion region spread is a function of applied voltage, resistivity, and impurity gradient.

The collector depletion region transit time (τ_m) is:

$$\tau_m = \frac{x_m}{2V_x} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (17)$$

where:

x_m = depletion region length

V_x = drift velocity of the minority carrier in the depletion layer.

The drift velocity V_x can be determined from the calculated magnitude of the accelerating field at given potentials and

data presented by Ryder.[7] Except at low collector voltages, this velocity is 9×10^6 cm/sec, the lattice-scattering-limited maximum drift velocity for mobile-charge carriers.

The collector depletion region transit time is voltage dependent since the depletion region width changes with voltage. Therefore, the evaluation of the collector depletion region transit time, under fixed bias conditions, does not yield a realistic picture. This is particularly true since the base transit time decreases with voltage while the collector depletion region transit time increases with voltage.

The collector depletion region transit time (τ_m) and the base transit time (τ_b) depends on collector voltage and the sum of these delay times are shown in Figure 5.

Calculations performed using 20, 6 and 3 ohm-centimeter material indicates that it is advantageous to use the 3 ohm-centimeter material because of the shorter total transit time and the high-current, low-voltage operation desired. The higher capacitance associated with the 3 ohm-centimeter material is a disadvantage. A comparison of these various resistivity materials is shown in Table II and illustrates that these transit times and parameters are within the requirements for 500 megacycle operation.

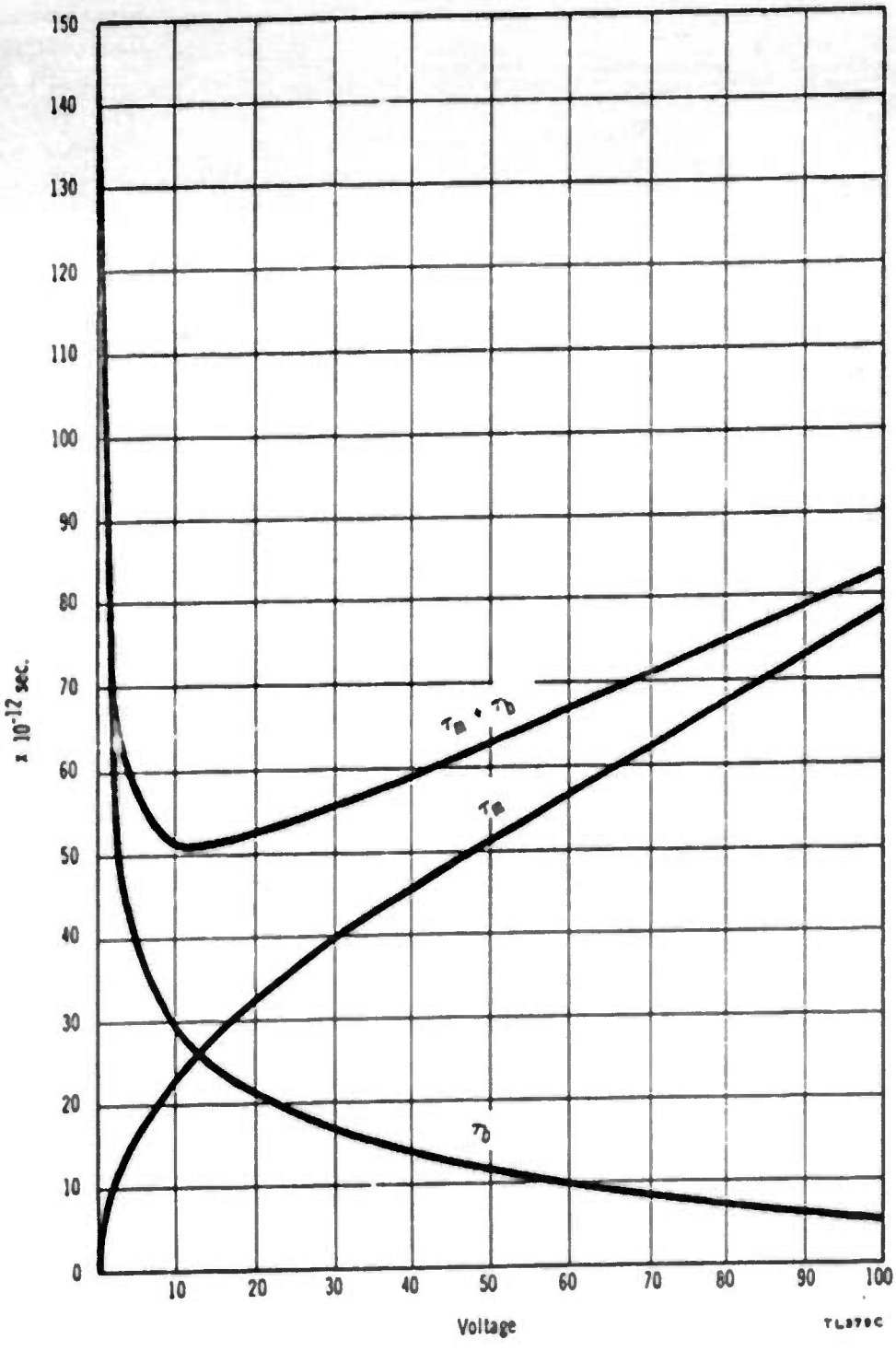


FIGURE 5 TRANSIT TIMES FOR COLLECTOR DEPLETION REGION (τ_m), BASE (τ_b), AND THEIR SUM ($\tau_m + \tau_b$)

TABLE II
COMPARISON OF VARIOUS RESISTIVITY MATERIALS
AT 28 VOLTS COLLECTOR POTENTIAL

Transit Time	Resistivity Materials		
	3 Ω-cm	6 Ω-cm	20 Ω-cm
Collector Depletion Region Transit Time (τ_m)	29.4×10^{-12} sec	43×10^{-12} sec	81×10^{-12} sec
Base Transit Time (τ_b)	26×10^{-12}	13.9×10^{-12}	7.3×10^{-12}
$\tau_m + \tau_b$	55.4×10^{-12}	56.9×10^{-12}	88.3×10^{-12}
Output Capacitance Common Base Configuration	4.9 pf	3.4 pf	2.3 pf
Emitter Transit Time τ_e	4×10^{-12}	4×10^{-12}	4×10^{-12}
Emitter to Collector Transit Time (τ_{ec})	5.94×10^{-11}	6.0×10^{-11}	9.2×10^{-11}

1. Design Consideration Summary

The general design considerations indicate optimums for each of the areas discussed. A summary of these results is presented in Table III.

TABLE III
SUMMARY OF DESIGN CONSIDERATIONS

Design Consideration	Material Consideration
Thermal Resistance	Large active collector area
V_{CBO}	High resistivity starting material and wide base width
V_{CEO}	High resistivity starting material and wide base width
V_{EBO}	High resistivity base dopant, long diffusion length
C_c	High resistivity starting material, small collector area
Current Gain	Long emitter periphery, narrow base width, low $r_{bb'}$
Low $r_{bb'}$	High dopant concentration in base region
Emitter Efficiency	High dopant concentration in emitter region
Large Gain Bandwidth (K)	Low $r_{bb'}$, C_c product, short τ_{ec}
Small τ_e	Small emitter area
Small τ_b	Narrow basewidth
Small τ_m	Low resistivity starting material

It can be seen from this table, that many of these requirements are conflicting. Therefore, it is necessary to evaluate the

relative importance of these design paremeters and establish compromises wherever possible.

Frequency considerations and thermal resistance are of fundamental importance since these determine the maximum operating frequency and approximate power levels. The expression for gain-bandwidth figure of merit (K) must be maximized. The base spreading resistance ($r_{bb'}$), collector capacitance (C_c), and emitter to collector transit time (τ_{ec}) must be kept small. These conditions dictate high base dopant concentrations, small emitter area, narrow base width and low resistivity starting material. Again, even within this same expression a compromise must be reached, narrow base width results in short base region transit time but higher values of $r_{bb'}$.

j. Limitations of Interdigitated Geometry

The operating current and, hence, the power output of a device, is dependent on emitter periphery. The required emitter periphery must be obtained using a minimum of emitter area. This area must be contained within a minimum of base area, so that emitter-base and collector-base junction capacitances are kept low, leading to both high efficiency and high gain. This can be accomplished by making the emitter and base fingers as narrow as possible. Thus, the width of metalization must be reduced and the resistance through the fingers rises, thereby

increasing IR drops which cause injection to fall off along the finger length. The results of a decrease in finger width can be compensated by an increase in metallizing thickness. However, photoresist and etching techniques impose a limit on the ratio of finger width to metal thickness.

A second limitation of the comb structure is the relatively large emitter area when compared to emitter periphery. This large emitter area is caused by the terminal strip used for bonding at the back of the emitter comb and by the limitation of emitter periphery to emitter area ratios. While it would be possible to substantially reduce this area, by extending the emitter bonding area out over the collector oxide, the area still remaining would be appreciable.

A third limitation on the use of comb type geometry is the impedance associated with the bonding wires and metallized fingers. Since small bonding areas and narrow emitter finger widths must be employed to reduce device capacitance, very small bonding wires and thin metallizing on the fingers is essential. This results in an increase in the resistive and inductive reactance components of the emitter impedance which raises the input resistance and consumes input power, thereby decreasing the power gain.

B. SURFACE GEOMETRY

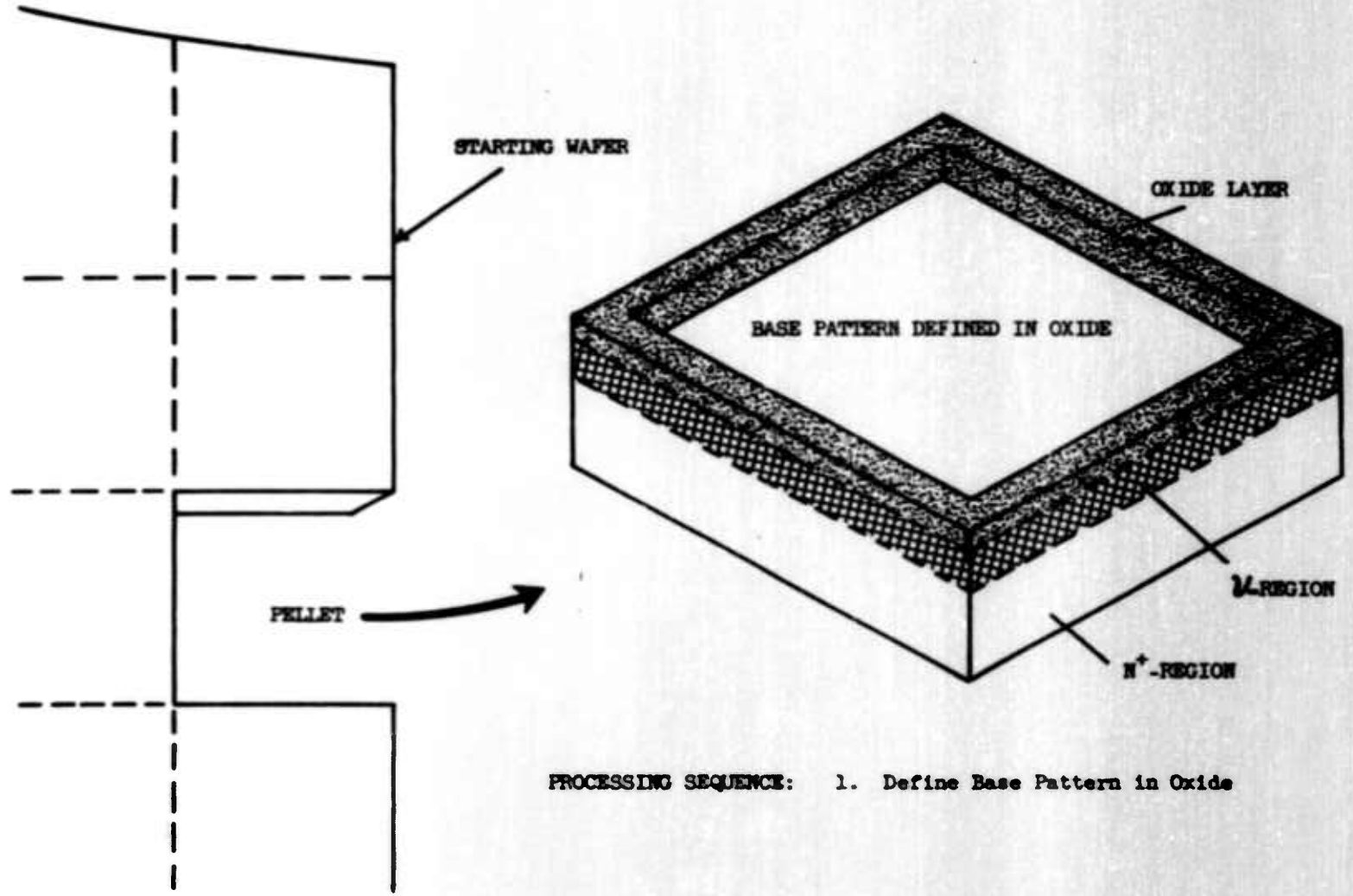
1. Overlay Structure

The three previously mentioned limitations on the comb type geometry can be overcome by the use of an overlay structure. The outstanding feature of this structure is the concept of emitter metallizing over both the base conductors and the emitter. This allows the emitter to be incorporated into the device in the best geometry for good frequency response and high current capability.

A pictorial representation of the formation of this device, as originally proposed, is shown in Figures 6 through 12.

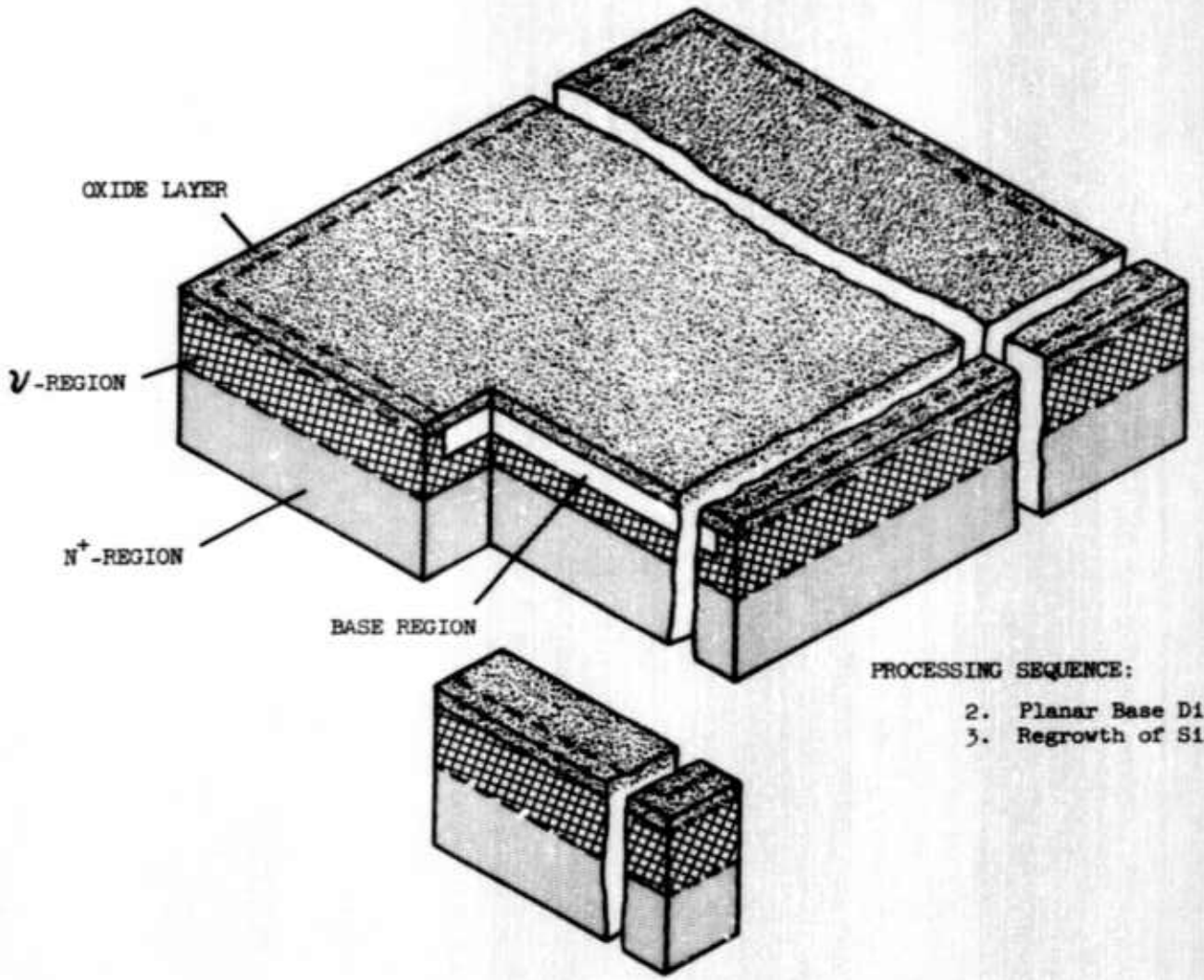
The base pattern illustrated in Figure 6 is the first photo-resist pattern applied. Following the base diffusion depicted in Figure 7, the emitter pattern is applied as shown in Figure 8. The emitters are small squares having a dimension of 0.5 mils per side with a separation of 1.4 mils. There are 156 emitter sites per device arranged in a 12 by 13 array.

Following the emitter diffusion (Figure 9), the units are ready for base metallizing. This is where the initial departure from standard processing occurs. The metallizing is performed in several steps rather than the usual two steps. The first step in the process is to remove the oxide by etching between the emitters and also inside of them, leaving the emitter-base junction and collector-base junction still covered by oxide as shown



PROCESSING SEQUENCE: 1. Define Base Pattern in Oxide

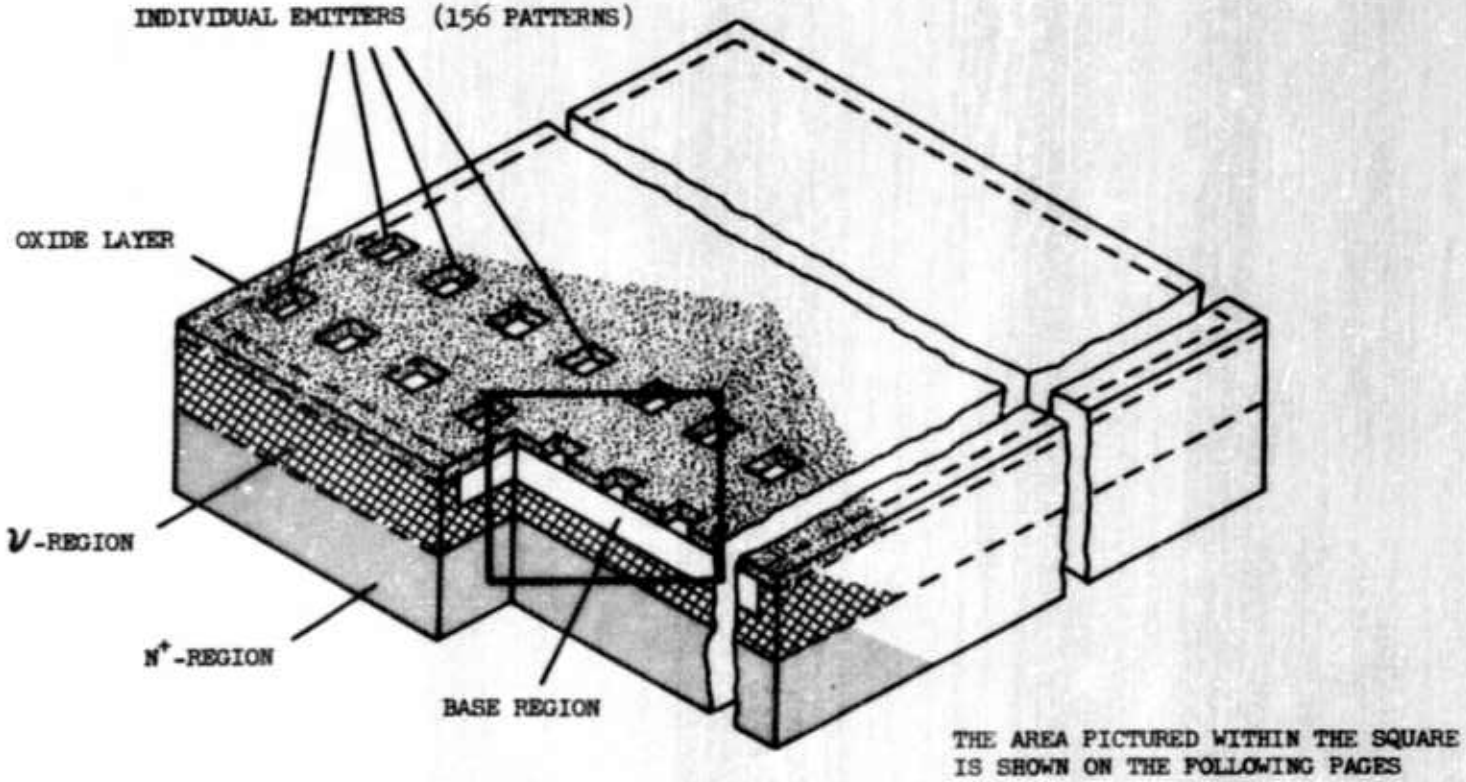
FIGURE 6 BASE PATTERN DEFINITION



PROCESSING SEQUENCE:

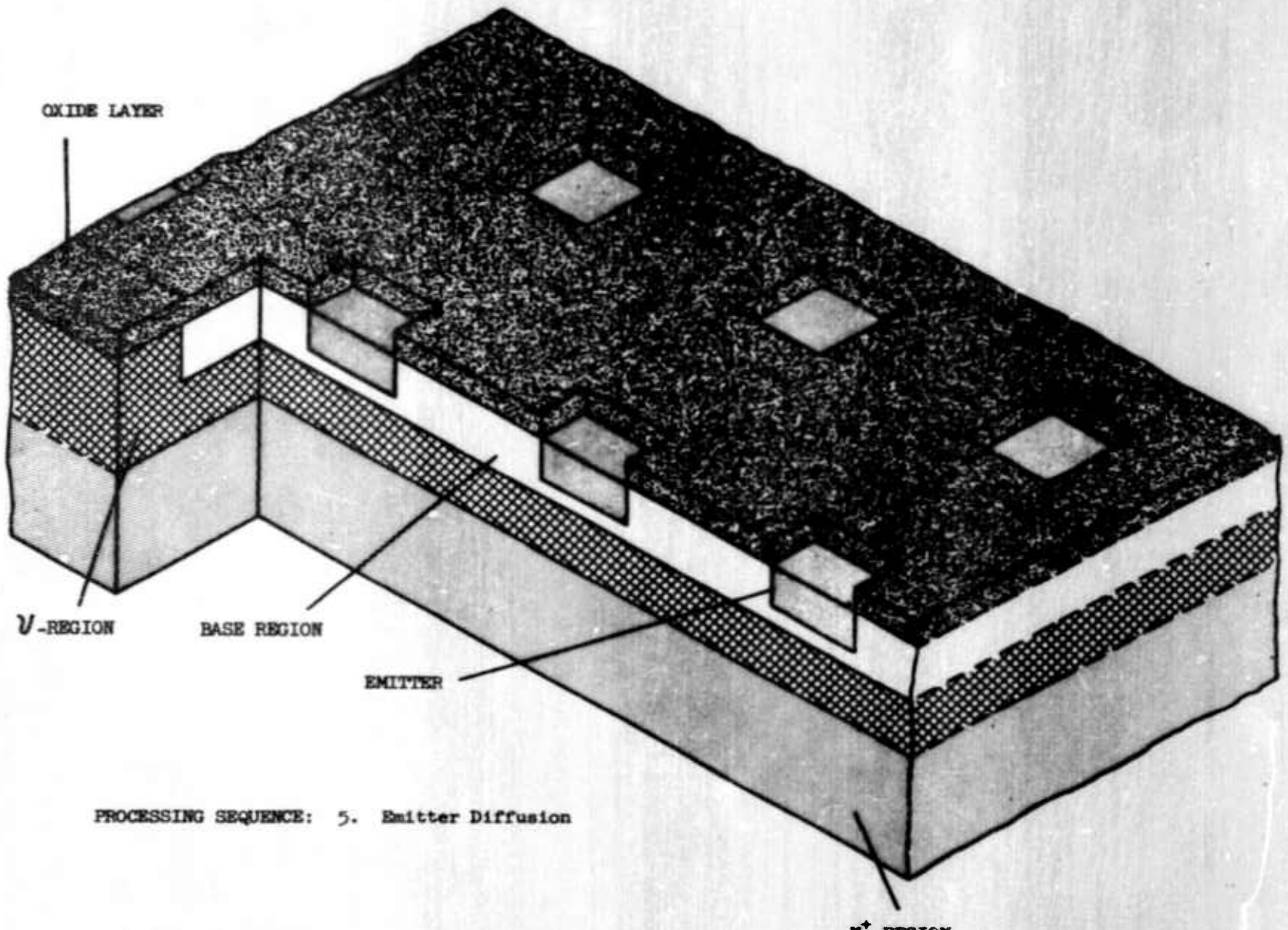
2. Planar Base Diffusion
3. Regrowth of Silicon Dioxide Layer

FIGURE 7 BASE DIFFUSION AND REGROWTH OF SILICON DIOXIDE LAYER



PROCESSING SEQUENCE: 4. Emitter Pattern Formation

FIGURE 8 EMITTER PATTERN FORMATION



PROCESSING SEQUENCE: 5. Emitter Diffusion

FIGURE 9 EMITTER DIFFUSION

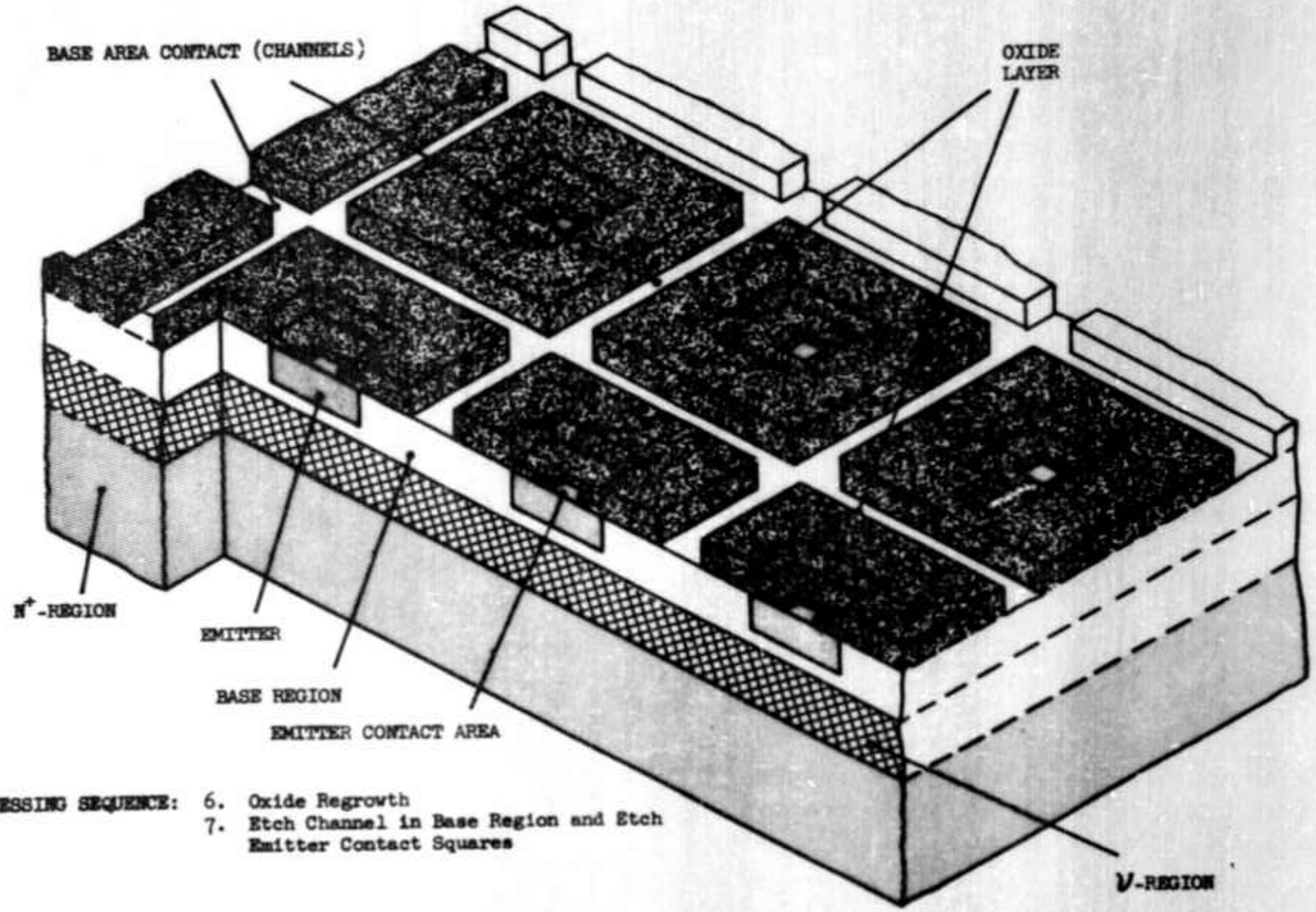


FIGURE 10 EMITTER OXIDE REGROWTH, ETCHED BASE CHANNELS, AND ETCHED EMITTER SQUARES

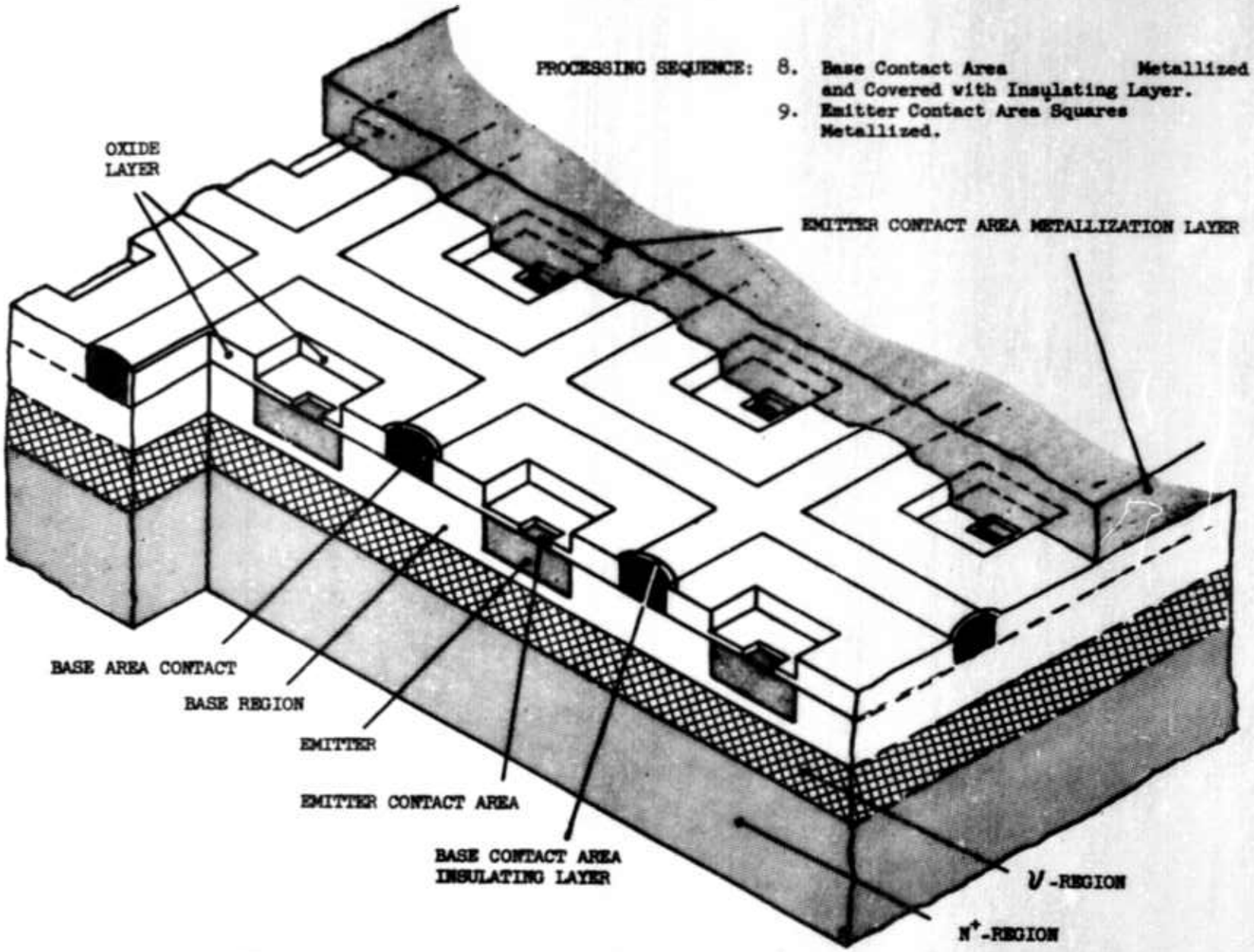


FIGURE 11 METALLIZED BASE CHANNELS BASE INSULATING LAYER AND METALLIZED EMITTER SQUARES

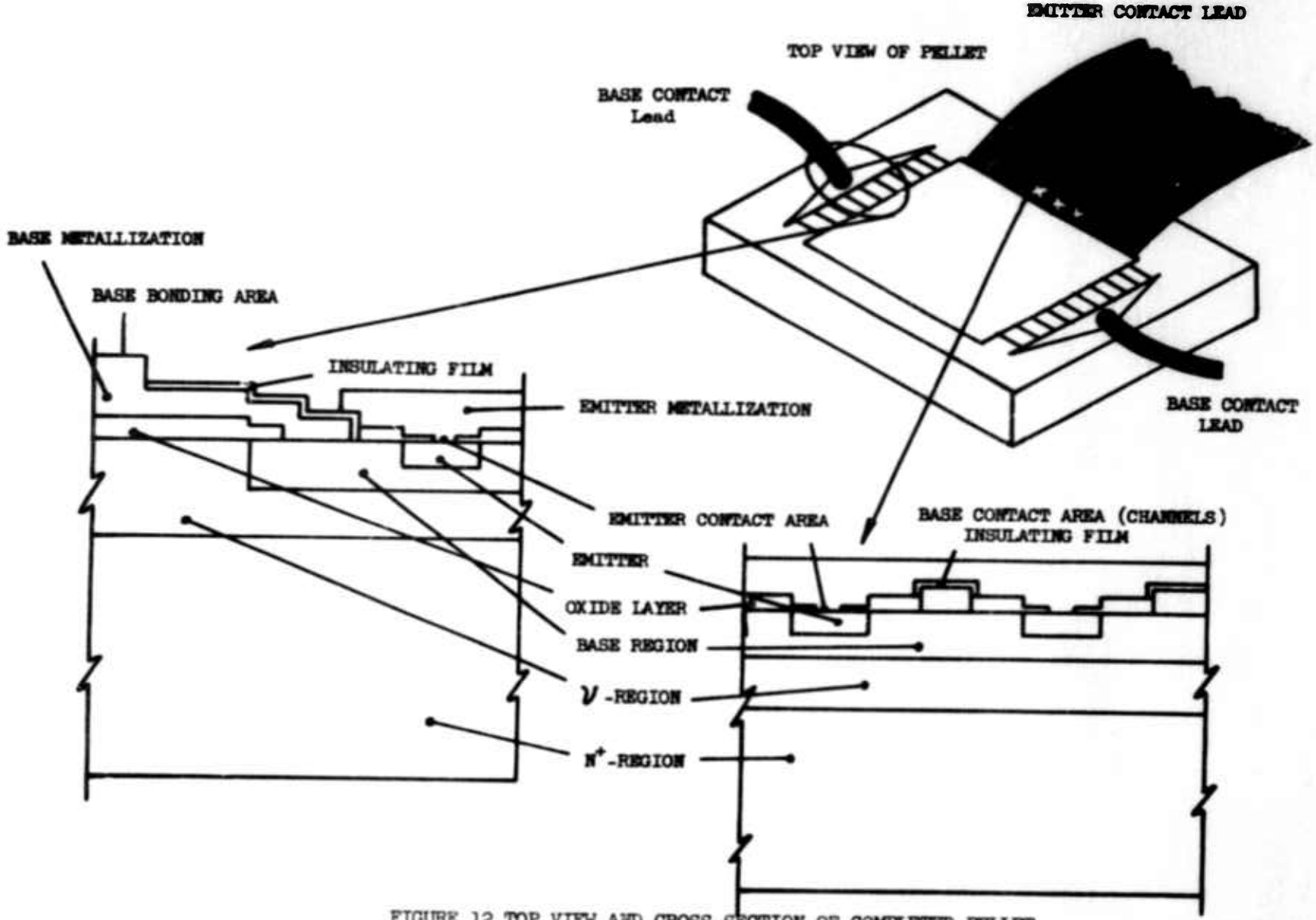


FIGURE 12 TOP VIEW AND CROSS-SECTION OF COMPLETED PELLET

in Figure 10.

Aluminum is then evaporated over the entire wafer to a thickness of 10,000 to 30,000Å. The base metallizing is then etched away so that the aluminum remains, not only in the base silicon areas between the emitters, but also extends over the oxide covering the collector base junction, terminating in the triangular areas where bonds are made as shown in Figure 12.

Following the aluminum evaporation, the base metallizing is covered by an insulating film (Figure 11), formed by anodizing the aluminum, or evaporating an insulating film such as a silicon oxide. In using silicon oxide, an extra step is required to etch the squares inside the emitter, shown in Figure 11, to remove the oxide from these areas. This step is not required using the anodized film approach.

After the insulating film is formed, contact is made to the emitters by evaporating 10,000 to 60,000Å of metal over the entire wafer. This new metal layer is defined over the entire device as shown in Figure 11.

2. Modified Overlay Structure

Difficulties associated with the fabrication of the insulating layer (Section C-2) led to the design of a "modified" overlay structure. This modified structure retains most of the advantages of the original structure but reduces fabrication problems by the introduction of a highly doped diffused P^+ matrix surrounding each emitter site. This conductive channel eliminates the need for metal conductors

over short lengths.

After the base diffusion cycle, the P^+ layer is diffused into the regions completely surrounding each of the future emitter sites as illustrated in Figure 13. An oxide layer is grown over the wafer and reopened in the emitter sites to accept the emitter diffusion as can be seen in Figure 14. After the emitter diffusion and oxidation, the reverse oxide pattern is opened allowing the evaporated aluminum film to make contact with the emitter and base contact areas. As depicted in Figure 15, each emitter site is opened in the form of a 0.3 mil square while only every other horizontal base contact stripe is opened. Conduction of base current from sides of the emitter not directly opposite a metallized base stripe is by means of the highly conductive P^+ layer parallel to these sides. The base current opposite these sides will flow through the lowest resistance path to the metallized base stripes. Calculation of the maximum voltage drop down the P^+ layer, based on the maximum base current, indicate the drop does not appreciably affect injection from these sides of the emitters.

Figure 16 shows a defined metal contact pattern. In this figure, the wider metal stripes make contact to the emitters through the oxide openings and are insulated from the base by thermally grown silicon dioxide.

The dimensions of the "modified" overlay structure device are shown

MAGNIFICATION 200X

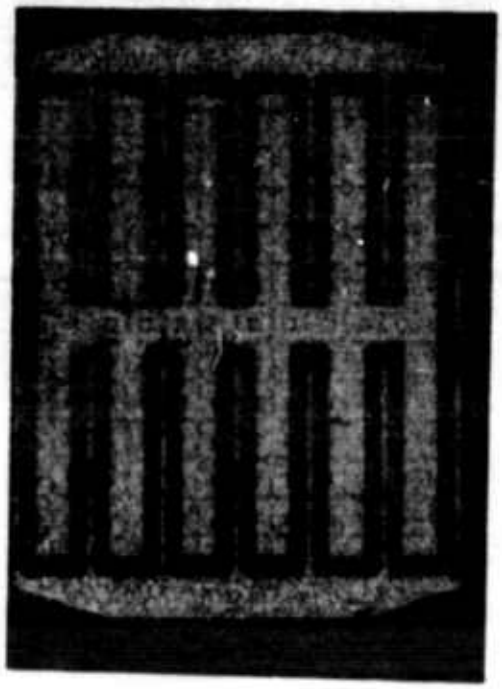
FIGURE 13 HIGHLY DOPED P MATRIX AFTER DIFFUSION INTO BASE REGION

MAGNIFICATION 200X

FIGURE 14 REGISTERED PHOTORESIST PATTERNS AFTER EMITTER DIFFUSION

MAGNIFICATION 200X

FIGURE 15 REGISTERED PHOTORESIST PATTERNS OPENING OF EMITTER BASE CONTACT AREAS



MAGNIFICATION 200X

FIGURE 16 DEFINED METAL CONTACT PATTERN

in Table IV and a comparison of these dimensions to a 3 watt, 150 megacycle comb type device is presented.

TABLE IV
DIMENSIONS OF MODIFIED OVERLAY GEOMETRY
(TA-2307)

Dimensions	Modified Overlay	Comb Structure 3w, 150mc
Total Base Area (BA)	380 square mils	1726 square mils
Emitter Area (EA)	39 square mils	657 square mils
Emitter Periphery (EP)	312 mils	438 square mils
Pellet size	50 x 50 mils	55 x 58 mils
EP/EA	8.0/mil	0.668/mil
EP/BA	0.826/mil	0.255/mil

The ratios EP/EA and EP/BA indicate the relative periphery in a given area and, as previously discussed, have a direct bearing on the current handling ability and maximum operating frequency of a device. It is apparent from Table IV that a significant improvement in the design ratios is realized with the modified overlay structure.

C. PROGRESS DEVELOPMENT

1. Mask Design and Fabrication

The importance of the transistor area in device theory has been shown in Section IV-B. In general, the best frequency response and power gain is obtained by minimizing the emitter and collector areas. Also, the spacing between the active emitter sites and

the length of metal contacts should be as small as possible.

The size and minimum tolerances in a device are determined by the precision of the masking and the ability to reproduce the mask pattern on the silicon wafers.

The masks for this device were designed with minimum line widths of 0.3 mils. The dimensions of the emitter diffusion and reverse oxide masks are such that the masks must align to within a tolerance of 0.1 mil. The specific mask patterns and dimensions along with the particular purpose of each mask are given in Figures 17 through 23.

The originally proposed mask patterns are given in Figures 17 through 20.

Figure 17 shows the base diffusion mask; the negative of this pattern, rotated 90°, was to be used as the emitter metallizing mask. Figure 18 shows the P^+ diffusion mask; the negative of this mask was to be used as the base metallizing mask. Figures 19 and 20 illustrate the emitter diffusion and silicon monoxide reverse oxide patterns, respectively.

The mask used in the fabrication of the modified overlay are depicted in Figures 21 through 23. The original base mask (Figure 17) and the original emitter mask (Figure 19) are used in this device. Figure 21 shows the modified P^+ diffusion mask. The reverse oxide pattern is shown in Figure 22 and the metallizing mask is illustrated in Figure 23.

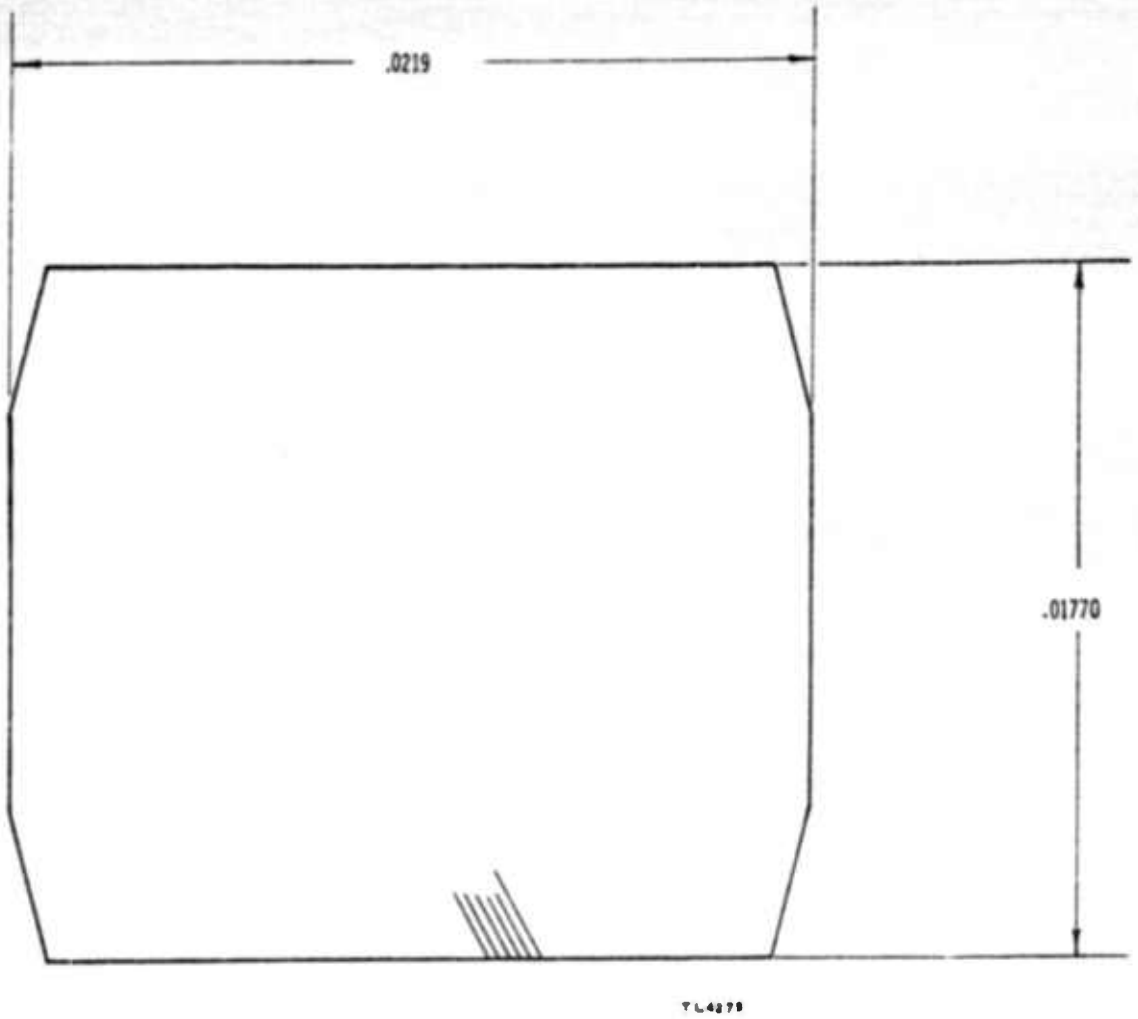


FIGURE 17 BASE DIFFUSION MASK

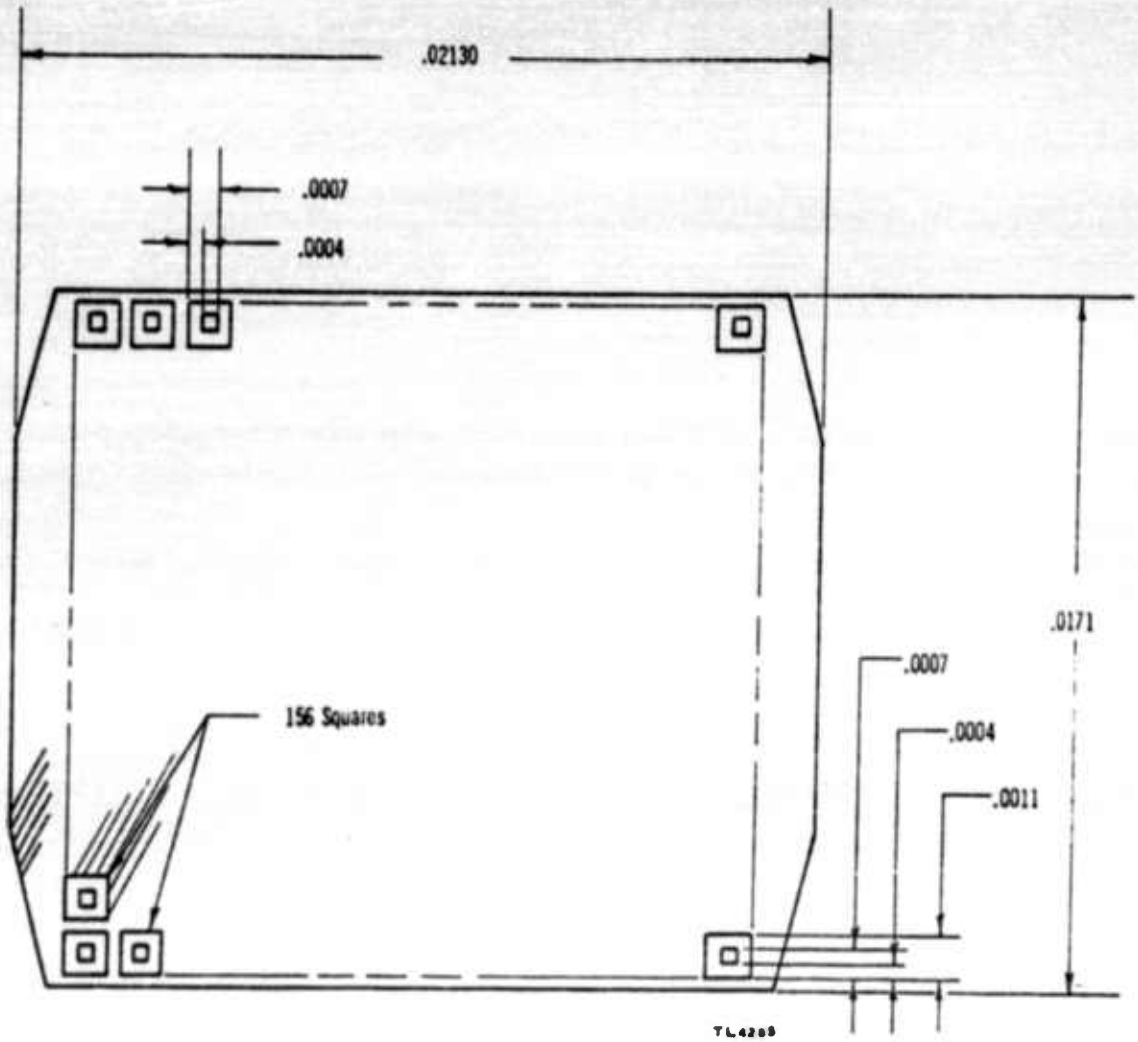


FIGURE 18 P+ DIFFUSION MASK

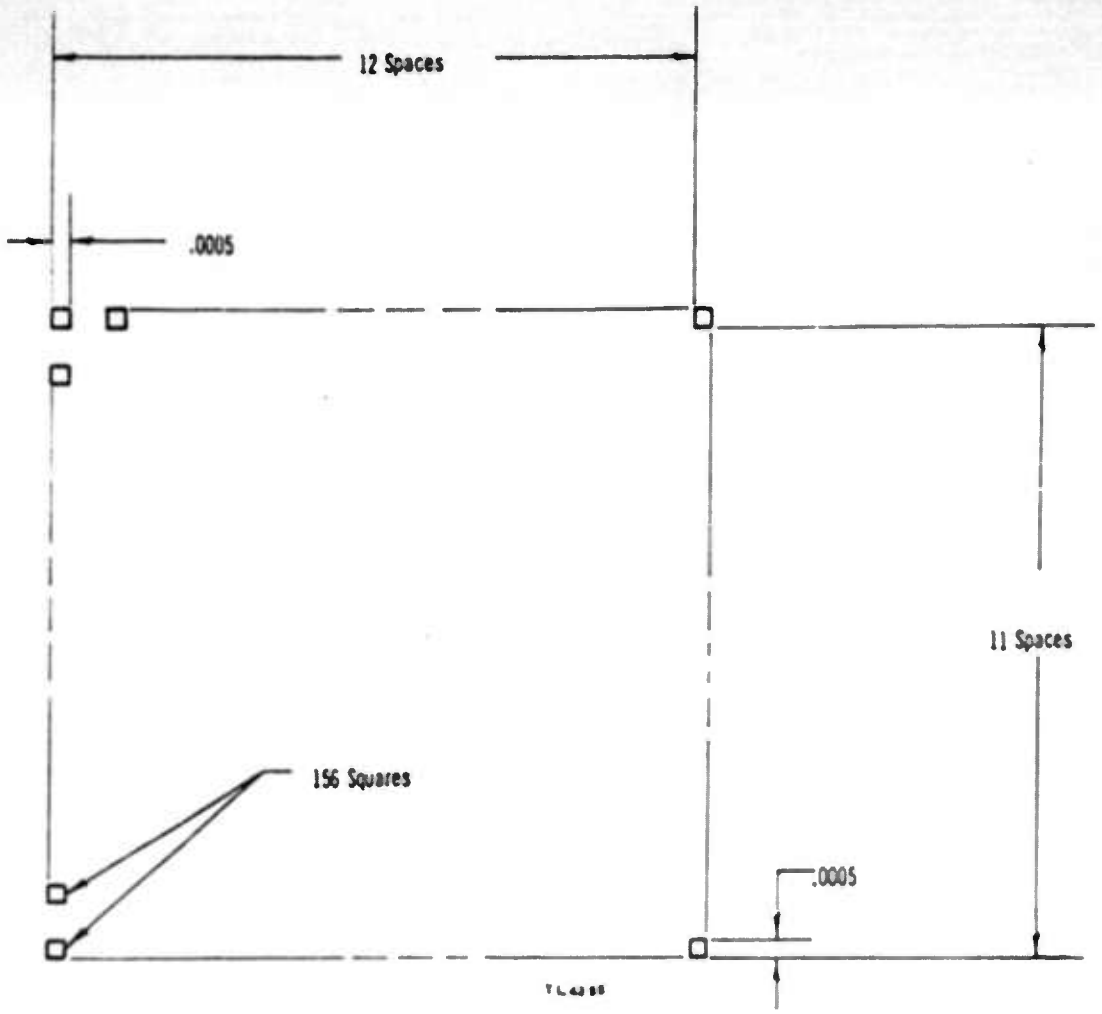


FIGURE 19 EMITTER DIFFUSION MASK

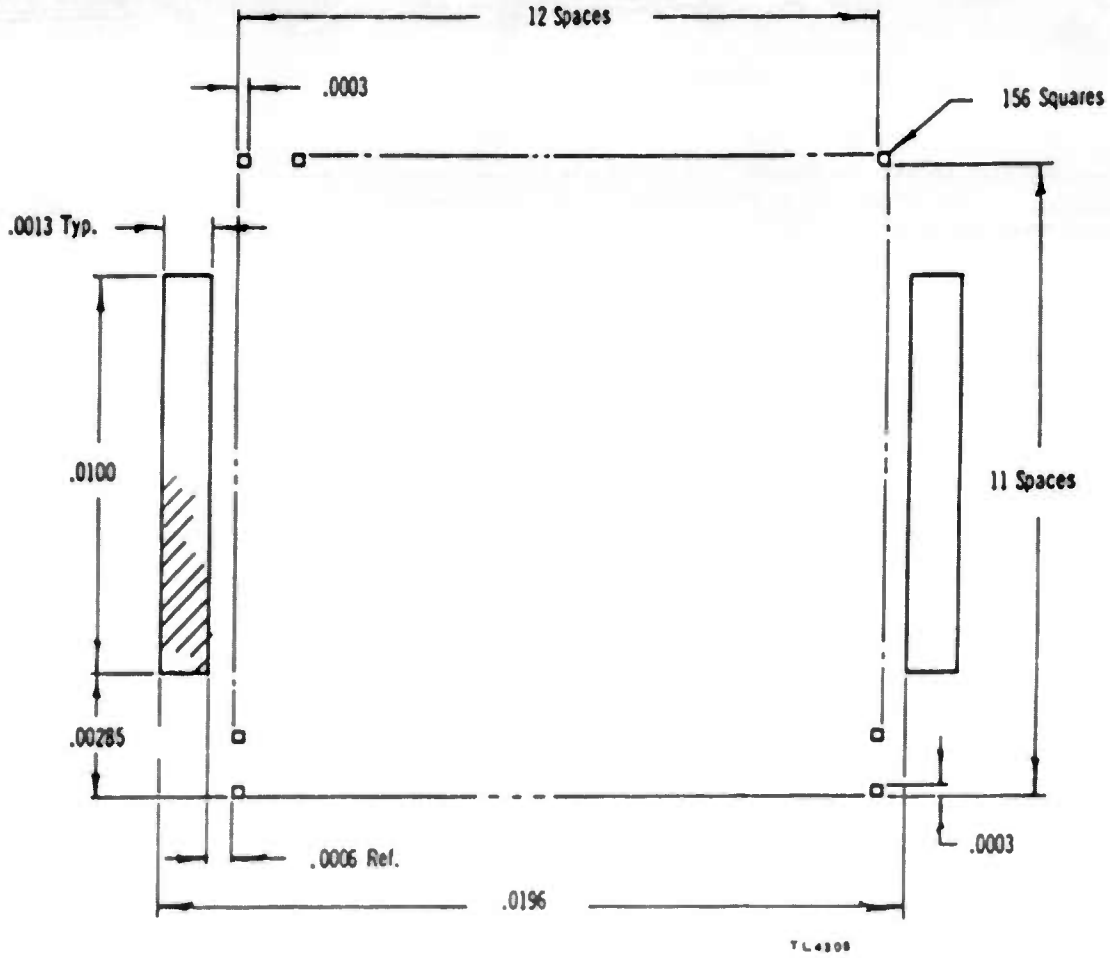


FIGURE 20 SiO REVERSE OXIDE MASK

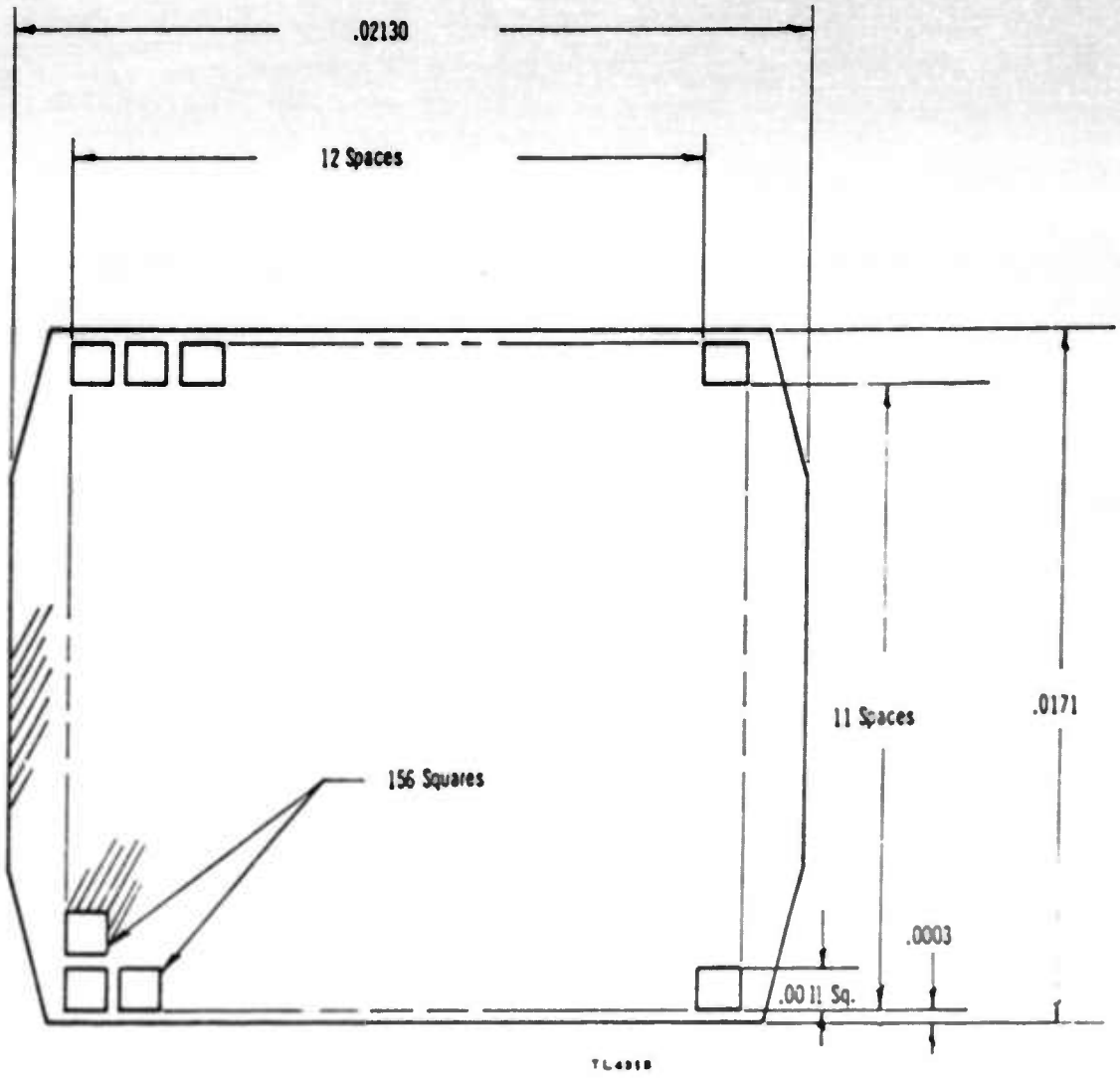


FIGURE 21 MODIFIED P+ DIFFUSION MASK

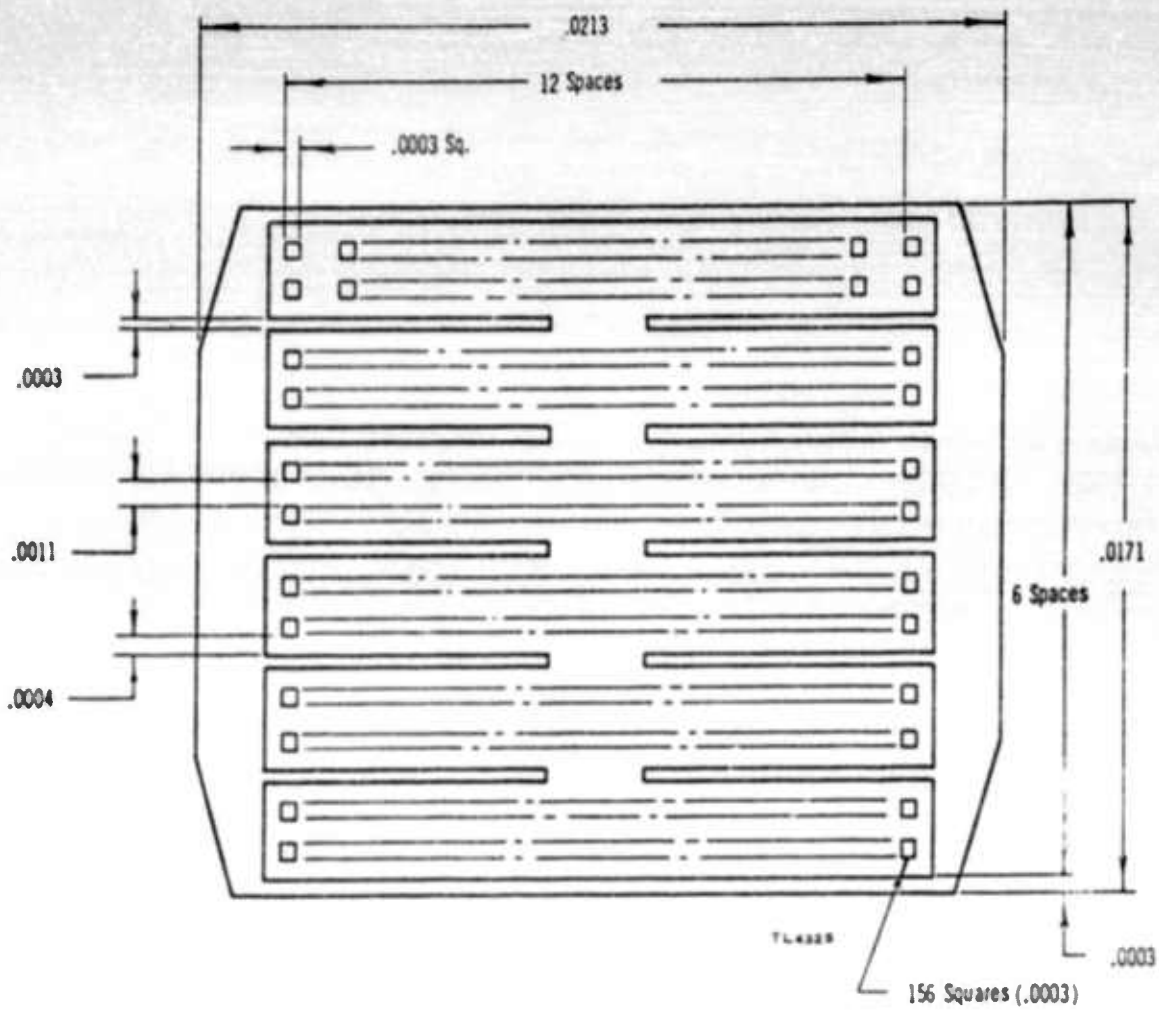


FIGURE 22 REVERSE OXIDE MASK

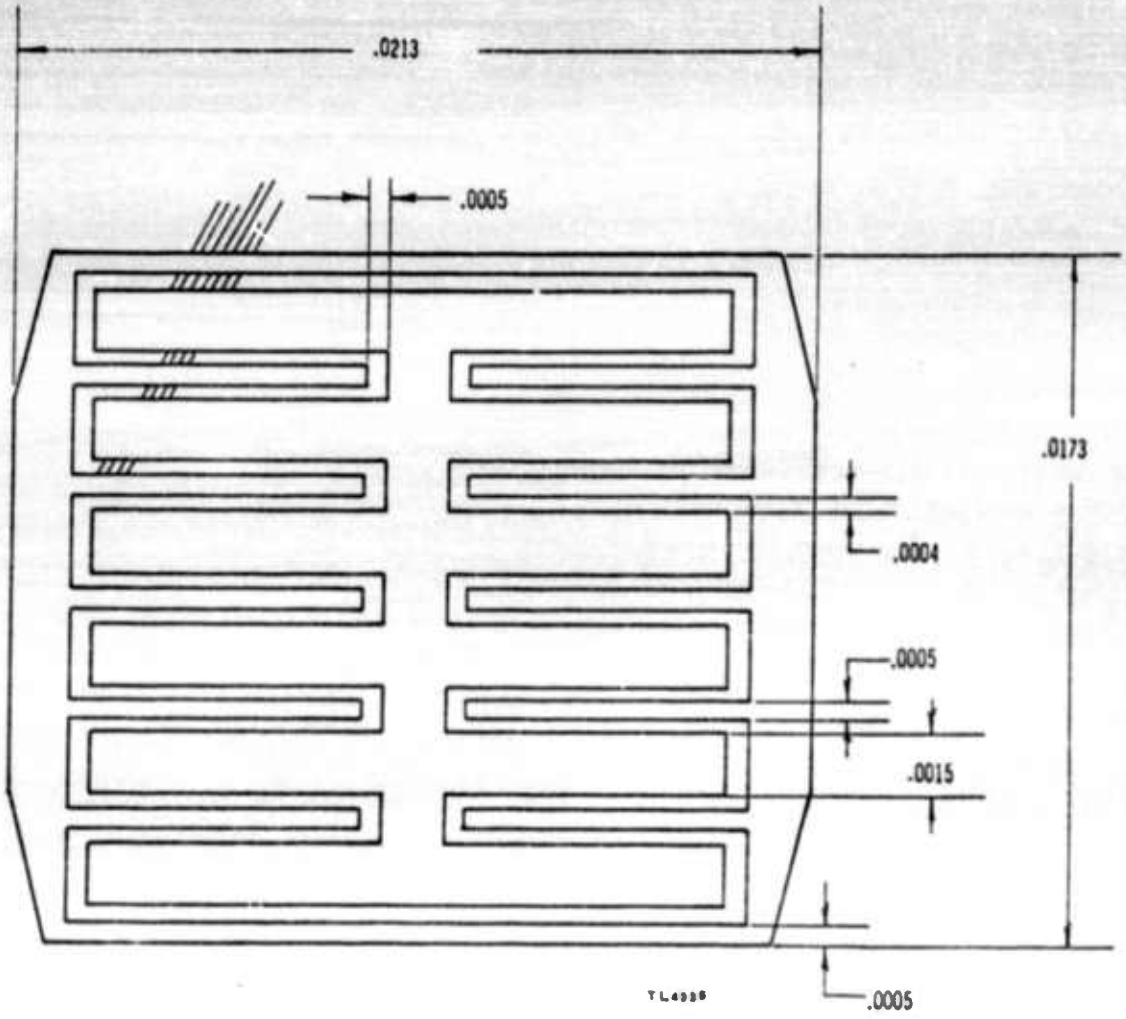


FIGURE 23 METAL CONTACT MASK

The extremely small geometry of this device necessitated the use of new photoresist mask fabrication techniques. Edge definition, maintenance of small radius corners, opaqueness, emulsion free clear areas and registration of the various masks were specific points of concern in the fabrication of these masks.

Samples were requested for the most difficult mask from several vendors including the RCA Photomask Laboratory. Evaluation of the various samples indicated the masks made by the RCA Photomask Laboratory were superior. Because of this, the Laboratory supplied subsequent masks required on the program.

2. Metal Over Metal Overlay (Insulating Layer)

For the fabrication of the originally proposed overlay structure, it is essential that the insulating film over the base metallizing have certain properties. These include: freedom from pinholes; strong adherence to the substrate material; offer very low leakage current; and the capability of being placed, formed or defined in particular areas in reasonable lengths of time.

Three basic systems for the fabrication of the insulating layer were investigated; evaporation of silicon monoxide over the entire surface and the definition of this film by photolithographic techniques, evaporation of silicon monoxide through a metal mask, and the anodic formation of an aluminum oxide layer on the surface of the base metallizing.

a. Photolithographic Definition of Silicon Monoxide

Initial studies on evaporated silicon monoxide films indicated that the properties of the film were largely dependent on the temperature of evaporation, source to target distance, substrate temperature and the vacuum system pressure. Difficulty was encountered in etching these films in reasonable lengths of time using ammonium bi-fluoride etching solutions. This may be caused by too high an evaporation temperature which results in the dissociation of the silicon monoxide source material into silicon and silicon dioxide. Measurements of the etch rate of films deposited at various source temperatures indicate the etch rates range from 130 to 180Å per minute. The fastest are attained at the slowest deposition rate, approximately 120Å per minute. The slow etch rate requires the defined photoresist to be exposed to the oxide etch for long periods of time and often resulted in failure of the resist to properly mask the substrate. The maximum allowable thickness of the silicon monoxide film is approximately 2500-3000Å since the photoresist affords protection for only about twenty minutes in oxide etch under the best conditions.

The slow evaporation rate resulted in films capable of having relatively large patterns (two mil stripes) defined in them. These films, approximately 2000Å thick, were extremely adherent to the substrate material, both the sili-

con areas and the thermally grown silicon dioxide regions. Further, they were not scratched or damaged when scraped with a stainless steel scribe.

Additional difficulty in the definition of the silicon monoxide insulating layer was encountered in the fabrication of an actual overlay device. In these studies, silicon monoxide was deposited over the entire wafer after the base metallizing had been completed. Photoresist techniques were employed in an attempt to define this insulating material so that the emitter contact areas were free of silicon monoxide while the metallized base matrix remained covered by the monoxide film. All attempts to fabricate a device using this procedure resulted in failure due to an inability to etch out the emitter contact areas. The failure mechanism consisted of a lifting of the photoresist in one to two minutes after immersion in the oxide etch, a failure of the photoresist to mask at the aluminum-silicon dioxide-silicon monoxide interface or a combination of these two mechanisms. Various substrate cleanup procedures, evaporation conditions and photoresist techniques were employed in unsuccessful attempts to eliminate this condition.

b. Metal Mask Evaporation of Silicon Monoxide

Attempts were made to fabricate an overlay structure tran-

sistor by the evaporation of silicon monoxide through a metal mask. A mask was designed with 0.7 mil slots and 0.7 mil spacing between them. A drawing of this mask is shown in Figure 24.

Two successive evaporations and placing the mask at right angles were required to cover the base metallizing grid. This approach allowed the deposition of the silicon monoxide only on the metallized base matrix after the emitter contact area had been opened and, therefore, did not require subsequent etching. However, difficulty was encountered due to a scattering of the evaporated silicon monoxide under the metal mask and because of the incidence of emitter base short circuits at the sharp edges of the metallized base matrix. The problem caused by the scattering was greatly reduced with the insertion of a shutter, having a small orifice, into the evaporation system between the source and target.

Further difficulties were encountered due to inadequate surface cleanup procedures after the silicon monoxide evaporation and prior to the emitter metallizing. This resulted in poor adherence of the metal film to the emitter contact area and consequently, devices exhibiting current gain only at very low current levels could be fabricated. Attempts to employ more rigorous surface cleanup procedures resulted in random destruction of the insulating layer.

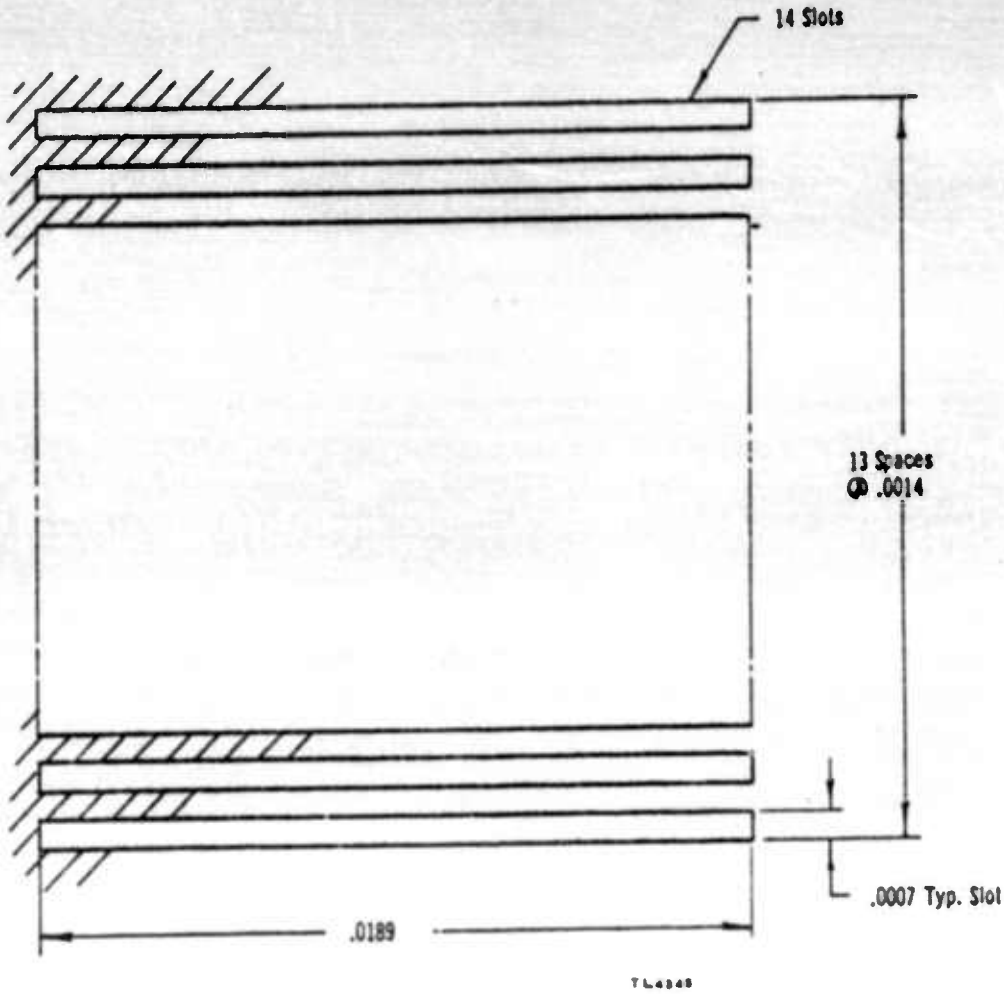


FIGURE 24 METAL MASK

c. Anodic Formation of Aluminum Oxide (Al_2O_3)

Another approach investigated for the insulating layer between base and emitter metallizing was the anodic formation of Al_2O_3 on the aluminum base matrix. This anodized film possesses all the necessary physical properties of the insulating layer.

Initially, a device having an interdigitated structure was used as the vehicle for the experimental work. The metallized emitter and base areas of these units were anodized to 150 volts using a current density of 14 milliamperes per square inch of aluminum surface area in a 3% tartaric acid solution having the pH adjusted to 5.5 by the addition of ammonium hydroxide.

The anodized layer on the metallized emitter was scribed open exposing the aluminum; a second metal film was deposited over the emitter and anodized base fingers using a metal mask evaporation technique. The anodized base metallizing area, which had an emitter metallizing overlay, was 1680 square mils, a factor of 15 greater than the proposed device. Measurement of V_{EBO} indicated 90 percent of the units were insulated.

Other experiments on comb type structures, modified into an overlay but without the aluminum oxide on the emitter metallizing scribed open, showed leakage currents between

the metallizing layers of only 5 nanoamperes at 60 volts.

Effort was then concentrated on the use of anodization using the patterns for the overlay device. These efforts were largely unsuccessful in so far as fabricating a device capable of the specified operating current. In general, the difficulty was in opening the emitter oxide, after anodizing the base metal, so that contact could be made to those areas during emitter metallizing. Specifically, the problem was poor adherence of the photoresist to the substrate due to inadequate surface cleanliness.

As in the case of the silicon monoxide, attempts to improve the adherence of the photoresist by the use of more thorough surface cleanup procedures resulted in the destruction of the anodic film.

An alternate technique to opening the emitter oxide was the use of a second metal evaporation. This evaporation followed the forming of Al_2O_3 on the base metallizing and was approximately 2000Å thick. It is known that this metal film adheres readily to the substrate with present surface cleanup procedures and that the photoresist adheres readily to the surface of this film. The photoresist was defined in the regions over the emitters and the metal film etched using conventional etching techniques. The wafers were then placed in oxide etch and this thin defined film was

used to mask the remaining areas of the wafers from the oxide etch, thereby allowing the opening of the emitter oxide.

The masking afforded by this thin film of aluminum was limited to approximately five minutes. The aluminum film was attacked by the oxide etch after this time and lateral etching under the defined aluminum "mask" occurred. This resulted in a total loss of definition of the contact area and consequently, this approach was discontinued.

During the initial phases of this contract, effort was expended on attempting to resolve the various difficulties associated with the originally proposed overlay structure. No reproducible, practical solutions to these technological problems were obtained. Because of these problems, the modified overlay structure was designed to eliminate the above fabrication difficulties.

3. Diffused Overlay Structure

The successful operation of the modified overlay structure depends to a large extent on the high degree of conductivity attainable in the P^+ matrix surrounding the emitter sites. This conductivity must be high enough that the voltage drop, caused by base current flowing through the matrix, does not seriously affect injection from any segment of an emitter site. This criteria required the

P^+ matrix to have the lowest possible sheet resistivity. Calculations based on a current gain of one and 156 emitter sites, each injecting uniformly, indicate a maximum voltage drop of approximately 40 and 4 millivolts in material having sheet resistances of ten and one ohms per square, respectively.

Experiments on attaining higher surface concentration in the P^+ matrix resulted in sheet resistivities almost two orders of magnitude lower than in the normal base region. This resistivity is low enough that the P^+ matrix can replace metal conductors for short distances and an insulating thermal silicon dioxide film can be grown over this layer.

As previously discussed in the section on device design, narrow base width (w) is essential for high frequency operation and increased current gain. Experiments were performed on the use of shallow base and emitter diffusions in an attempt to improve the control of the base width. Wafers were processed with a base penetration of 0.065 mil and an emitter penetration of 0.035 mil, yielding a base width of 0.03 mil.

More recent experiments resulted in control of the base width to 0.02 mils. Studies were performed on various resistivity starting material. These studies were conducted using identical diffusion depths in the different materials.

Evaluation of the optimum starting material was based on the output power delivered in the UHF power gain test set, described

in Section D-5 of this report. A comparison of devices fabricated on 6-9 ohm-cm and 3-4 ohm-cm starting material can be seen from the data in Table V.

It is apparent from this table that the lower resistivity material yields considerably more output power than the 6-9 ohm-cm material.

On the basis of the theoretical calculations and experimental studies, it was decided that the units would be fabricated on 3-4 ohm-cm starting material employing shallow diffusions.

The diffusion profile and junction depths of the final samples are illustrated in Figure 4.

4. Metallizing

Calculation of the bias voltage caused by IR drops along the base and the emitter metallized fingers indicates that this voltage drop is negligible for aluminum films 15,000Å thick using the modified overlay geometry. State-of-the-art metallizing techniques were applicable to the new device geometry and no refinement in this process was necessary.

5. Photoresist Techniques

The minute dimensions of this device imposed serious limitations on the alignment fixtures associated with the photolithographic processes. The dimensions necessitated the redesign of these fixtures so that

TABLE V
POWER GAIN COMPARISON OF STARTING RESISTIVITY MATERIAL

400 Megacycle Measurements of TA-2307
Common Emitter Configuration

Unit No.	Resistivity ohm-cm	P_{in} Watts	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
25-2	6-9	1.0	50	175	4.7	6.7	54
26-2	6-9	1.0	50	180	4.7	6.7	52
26-4	6-9	1.0	50	200	5.1	7.1	51
26-5	6-9	1.0	50	180	4.8	6.8	53
26-10	6-9	1.0	50	160	4.4	6.4	55
26-11	6-9	1.0	50	200	5.0	7.0	50
31-2	3-4	1.0	50	190	5.4	7.3	57
31-3	3-4	1.0	50	220	5.3	7.2	48

the wafer position, relative to the mask, could be controlled to within 0.1 mil. A metallurgical microscope was adapted to be used as the optical system in conjunction with this alignment jig.

Experiments in the definition of patterns indicated the necessity of an improved coating procedure for the application of the photoresist. Using normal whirling techniques, a pileup of photoresist approximately 0.1 mil high could be detected around the periphery of the coated wafers. This lip of material prevented close contact between the photoresist mask and the coated wafer during exposure. This resulted in a decrease in pattern definition and at times totally inadequate definition as depicted in Figure 25. This figure shows the difference in definition between wafers with and without the edge pileup. The photoresist pileup was eliminated by use of edge whirling. In this operation, the wafer is placed away from the center of the whirler instead of placing the wafer in the center. This results in eccentric revolution of the wafer and consequently, pileup around the entire edge of the wafer cannot occur. Since the alignment system incorporates a pivoting wafer holder, the pileup is compensated. Investigations of photoresist coating techniques, exposure time and developing techniques were performed to optimize the photoresist procedure. These studies indicated that the degree of pattern sharpness was not only affected by the position of the wafer on the whirler, but by the whirling speed and the photoresist thickness.

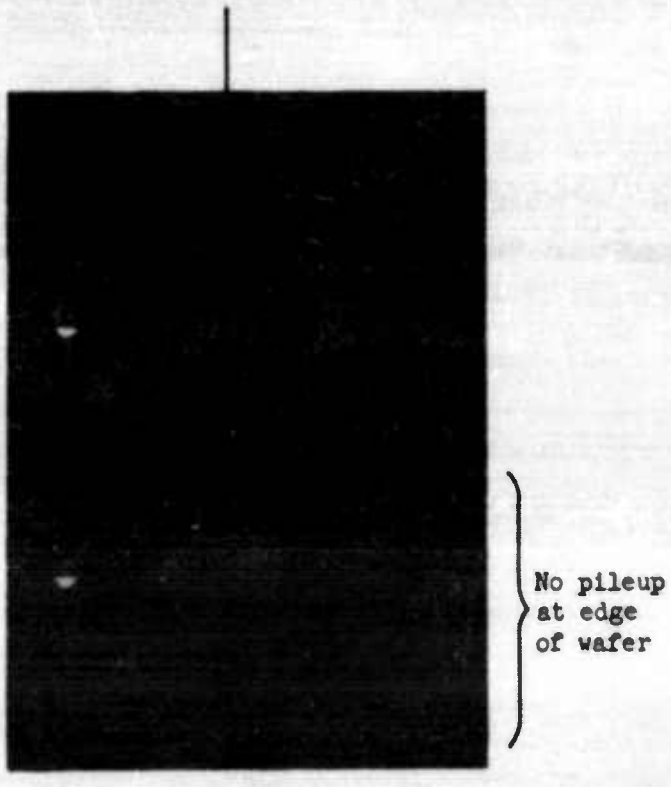


FIGURE 25 EFFECT OF RIDGE OR PILEUP OF PHOTORESIST AT EDGE OF WAFER ON PATTERN DEFINITION

Further, the length of time that the photosensitive emulsion is exposed greatly affects pattern sharpness. Too short or too long an exposure time leads to uncontrolled dimensions in the defined pattern.

The intensity of the light source also influences the degree of sharpness attainable. The optimum exposure conditions were determined by extensive examination of patterns exposed under various conditions and an optimum time was established for each lamp employed.

Developing techniques were examined in order to further improve definition of patterns. Various developing solutions were investigated such as trichlorethylene, KPR Developer and alcohol.

Because of these studies, advances in the state-of-the-art were realized. The degree of pattern sharpness was shown in Figures 13 through 15. As previously mentioned, Figure 13 shows the highly doped P^+ matrix after diffusion into the base region. Figure 14 illustrates the registered photoresist pattern after emitter diffusion, each small square being 0.5 mil on a side. The defined and etched reverse oxide pattern is depicted in Figure 15. In this figure, the emitter contacts are the small lightly shaded areas within the emitter sites. These contact areas are 0.3 mil on a side. A defined metal film approximately 30000Å thick is shown in Figure 16.

These figures indicate the degree of sharpness now attainable

using these recent advances in photolithographic techniques. The resolution is not determined by any one step in the process. All the phases are interdependent; the coating, exposure, development and baking must be optimized as a group.

D. DEVICE EVALUATION

1. Direct Current Parameters

A Tektronix Type 575 Transistor Curve Tracer was used to measure the static forward current transfer ratio (h_{FE}), saturation voltage $V_{CE}(sat)$, sustaining voltage (LV_{CER}), collector-base breakdown voltage (V_{CBO}) and the collector cutoff voltage (V_{CEO}).

Other direct current parameters were measured using a Keithley 610A Electrometer. These parameters include:

$$I_{EBO} \text{ at } V_{EBO} = 4V$$

$$I_{CBO} \text{ at } V_{CBO} = 40V$$

$$I_{CES} \text{ at } V_{CES} = 40V$$

Collector capacitance (C_{ob}) at a collector voltage of 40 volts was measured on a Boonton Model 75A-S8 Capacitance Bridge.

Table VI lists the direct current parameters of the experimental model transistors delivered.

Tables VII and VIII list the direct current parameters of the final two hundred transistors delivered during this contract. Table VII

is data on twenty units delivered prior to the required delivery date while Table VIII shows data on the later 180 final samples.

The collector cutoff current (I_{CES}) is measured using a Keithley Instruments Model 610A Electrometer and an Electronic Research Associates Model 210 transistorized power supply. A low leakage socket is used for the device measurements. The small amount of socket leakage current is compensated in the meter deflection prior to the measurements. The Keithley Electrometer has an accuracy of 1 percent and the direct current voltmeters used to monitor the source are also calibrated within one percent.

Figure 26 shows a distriubtion of the collector cutoff current (I_{CES}) at a collector voltage of 40 volts. It can be seen from this curve that 75 percent of the final units had collector cutoff currents less than the objective of 100 microamperes.

A distribution of V_{CE}(sat) at a collector current of 750 milliamperes and a base drive current of 140 milliamperes is shown in Figure 27. The value of V_{CE}(sat) was measured on a calibrated Tektronix Model 575 transistor curve tracer by the introduction of seven base generator steps of 20 milliamperes each.

The sustaining voltage (LV_{CER}) at a collector current of 50 milliamperes direct current through a collector circuit resistance of 10 ohms is presented in Figure 28.

The collector capacitance (C_{ob}) measured at a collector potential of 40 volts is shown in Figure 29. This capacitance is measured

TABLE VI
DIRECT CURRENT PARAMETERS ON EXPERIMENTAL MODEL TRANSISTORS

Experimental Model Transistor Delivery Number 1

Unit No.	I_{CEO} 75V μa	I_{CES} 28V μa	I_{CES} 75V μa	I_{EBO} 5V μa	LV_{CER} I_C=50ma R=100 Volts	h_{FE} V_{CE}=10V I_C=350ma	$V_{CE}(sat)$ I_B=150ma I_C=700ma Volts	C_{ob} 28V μμf
1	3.6	0.58	0.8	0.2	110	112	0.28	5.37
2	0.05 (60V)	0.012	.015 (60V)	0.2	100	175	0.24	5.42
3	0.009	0.005	0.007	0.7	100	140	0.25	5.50
10	64 (60V)	1.05	1.05 (60V)	0.2	98	200	0.24	5.74
11	0.18	0.035	0.04	0.2	110	200	0.25	5.45
12	.0005	.0001	.0004	0.2	110	219	0.25	5.46

Experimental Model Transistor Delivery Number 2

Unit No.	I_{CEO} 75V μa	I_{CES} 28V μa	I_{CES} 75V μa	I_{EBO} 5V μa	LV_{CER} I_C=50ma R=100 Volts	h_{FE} V_{CE}=15V I_C=35ma	$V_{CE}(sat)$ I_C=700ma I_B=140ma Volts	C_{ob} 28V μμf
1	.0003	.0006	.001	135	140	90	0.12	14.9
3	9000	95.0	170	54	120	80	0.14	15.5
12	.004	.0015	.004	88	135	80	0.15	13.6
13	.004	.001	.003	120	130	120	0.14	13.8
15	1.4	.09	.30	115	180	145	0.14	14.0
16	500	.25	.30	100	120	45	0.15	13.9
20	135	5.6	11	105	170	120	0.14	13.7

Experimental Model Transistor Delivery Number 3

Unit No.	V_{CBO} 100μa Volts	I_{CBO} 28V Ax10^{-9}	V_{CEO} (sus) Volts	V_{CEX} 100μa Volts	V_{EBO} 100μa Volts	V_{EBF} 1.0A Volts	h_{FE} 100ma 4V	h_{FE} 1.0A 10V	$V_{CE}(sat)$ I_C=.75A I_B=.14A	C_{ob} 28V pf
25-2	125	0.30	150	125	5.5	-	11	5	2.0	5.9
26-2	80	0.50	95	72	5.2	1.15	40	10	1.2	5.45
26-4	70	0.36	75	60	1.4	1.2	42	14	0.95	5.48
26-5	74	100	100	65	5.1	1.5	83	14	0.8	5.33
26-10	80	0.66	105	82	4.6	1.2	71	13	0.7	5.51
26-11	65	1.2x10^{3}	90	70	5.0	1.3	71	13	0.95	5.21

TABLE VII
DIRECT CURRENT PARAMETERS OF FINAL TA-2307 TRANSISTORS

Final Transistor Delivery Number 1

Unit No.	V_{CBO} 100μa Volts	I_{CBO} 75V ma	I_{CBO} 28V Amps	V_{CE} (sus) Volts	V_{CEX} 100μa Volts	V_{EBO} 100μa Volts	h_{fe} 100ma 4V	h_{fe} 1.0A 10V	$V_{CE\ sat}$ I_C=.75A I_B=.14A Volts	C_{ob} 28V pf
37-27	65	5.0	2.9×10^{-8}	88	50	5.0	8.0	9.5	2.5	8.79
34-13	70	0.001	1.8×10^{-10}	90	70	5.5	14.3	12.0	1.5	6.34
41-34	70	5.0	4.2×10^{-8}	78	60	5.0	7.7	14.2	1.1	8.28
34-19	80	0.001	1.6×10^{-10}	80	79	5.0	14.5	11.1	2.0	6.44
37-30	62	0.20	9.0×10^{-7}	95	60	4.0	7.7	8.35	3.0	7.25
37-33	65	1.0	1.9×10^{-4}	82	15.5	5.0	7.4	6.25	1.3	8.86
34-18	82	0.001	1.8×10^{-10}	97	80	5.0	16.7	11.1	2.1	6.70
37-9	80	0.06	1.1×10^{-5}	80	73	5.0	18.8	14.2	2.5	6.88
37-7	70	1.5	1.3×10^{-5}	95	35	4.0	28.3	18.2	1.4	6.83
41-33	68	4.0	1.4×10^{-7}	80	68	5.0	5.5	12.5	1.3	8.15
37-9	50	8.0	4.8×10^{-6}	82	14	5.0	22.1	16.7	1.7	7.15
41-32	53	—	2.4×10^{-7}	70	53	5.0	9.1	14.7	0.6	8.15
41-27	57	2.0	2.2×10^{-6}	80	48	5.0	38.2	9.1	1.8	7.66
34-9	80	0.001	1.0×10^{-9}	100	80	5.0	29.4	16.7	2.2	7.15
31-3	75	0.04	1.3×10^{-9}	95	70	5.1	25.0	8.35	1.6	5.90
37-23	70	0.1	8.3×10^{-9}	90	70	5.0	6.9	8.3	3.1	7.17
34-1	90	.04	2.2×10^{-10}	100	90	1.4	12.0	8.3	2.0	6.50
26-31	98	.07	2.2×10^{-8}	140	82	4.0	33.0	10.0	1.1	5.12
30-20	80	.08	1.4×10^{-6}	110	50	6.0	16.0	12.5	0.6	5.39
34-42	71	.12	2.1×10^{-8}	115	48	4.9	40.0	14.3	1.4	6.60

TABLE VIII

DIRECT CURRENT PARAMETER OF FINAL TA-2307 TRANSISTORS

Final Transistor Delivery Number 2

Unit No.	V_{CBO} 100μa Volts	V_{CEO} 100μa Volts	I_{EBO} 4V Amperes	I_{CBO} 40V Amperes	I_{CES} 40V Amperes	LV_{CER} 50ma R-10Ω	h_{FE} V_{CE}-10V I_C-350ma	$V_{CE}(sat)$ I_C-750ma I_B-140ma	C_{OB} 40V μμf
37-20	70	11	4.8×10^{-6}	2.9×10^{-6}	3.9×10^{-4}	91	14.0	1.2	6.88
37-22	52	42	4.8×10^{-6}	2.1×10^{-8}	1.2×10^{-5}	90	13.5	1.1	7.0
37-25	61	27	6.8×10^{-6}	1.6×10^{-6}	1.4×10^{-4}	90	7.8	1.6	7.58
37-28	44	22	8.6×10^{-4}	9.7×10^{-5}	2.1×10^{-4}	95	9.2	1.55	7.63
37-29	68	65	5.8×10^{-6}	1.2×10^{-7}	2.3×10^{-5}	102	7.0	2.4	6.63
40-11	80	80	4.0×10^{-3}	6.2×10^{-11}	6.2×10^{-11}	100	10.9	1.2	7.07
40-14	76	76	4.2×10^{-7}	1.8×10^{-9}	1.8×10^{-9}	94	12.7	1.15	7.23
40-21	76	76	1.4×10^{-6}	1.2×10^{-10}	1.2×10^{-10}	100	16.1	1.0	7.1
40-28	60	35	5.7×10^{-7}	2.8×10^{-5}	1.6×10^{-4}	85	10.9	1.2	7.24
41-1	60	60	4.6×10^{-6}	2.2×10^{-9}	2.2×10^{-9}	71	11.3	1.1	7.7
41-2	65	65	6.0×10^{-7}	4.2×10^{-9}	4.1×10^{-9}	82	12.5	1.0	7.26
41-4	65	65	4.4×10^{-6}	5.2×10^{-9}	3.0×10^{-6}	80	8.7	1.5	7.9
41-8	68	68	4.2×10^{-6}	3.4×10^{-9}	3.4×10^{-9}	82	6.8	2.6	6.9
41-9	55	55	9.8×10^{-7}	2.3×10^{-9}	2.3×10^{-9}	71	6.8	3.0	6.25
41-10	43	15	6.7×10^{-6}	3.8×10^{-5}	2.4×10^{-4}	78	11.7	1.6	7.56
41-53	80	40	4.2×10^{-6}	8.0×10^{-8}	8.2×10^{-5}	105	21.8	.7	7.6
41-67	75	25	3.7×10^{-6}	2.2×10^{-7}	1.7×10^{-4}	100	17.5	.49	7.57
41-76	69	25	6.0×10^{-6}	6.4×10^{-6}	1.6×10^{-4}	90	14.0	.7	6.75
41-92	32	16	4.4×10^{-6}	1.5×10^{-4}	3.4×10^{-4}	89	23.0	1.4	7.19

TABLE VIII (Cont.)

DIRECT CURRENT PARAMETER OF FINAL TA-2307 TRANSISTORS

Final Transistor Delivery Number 2

Unit No.	V_{CBO} 100μa Volts	V_{CEO} 100μa Volts	I_{EBO} 4V Amperes	I_{CBO} 40V Amperes	I_{CES} 40V Amperes	LV_{CER} 50ma R-10Ω	h_{FE} V_{CE}-10V I_C-350ma	V_{CE}(sat) I_C-750ma I_B-140ma	C_{OB} 40V μμf
42-5	61	17	4.1×10^{-6}	1.4×10^{-6}	2.0×10^{-4}	79	23.1	.85	8.11
42-6	58	20	7.2×10^{-7}	8.2×10^{-8}	2.1×10^{-4}	75	25.0	.73	8.13
42-16	60	21	9.0×10^{-6}	3.5×10^{-6}	2.4×10^{-4}	72	13.4	1.0	8.19
42-19	60	21	5.8×10^{-6}	1.4×10^{-5}	2.0×10^{-4}	75	9.7	1.2	8.54
42-22	50	7.0	6.6×10^{-6}	5.8×10^{-5}	1.4×10^{-4}	70	6.7	.9	10.05
42-29	58	28	5.9×10^{-6}	2.3×10^{-6}	1.3×10^{-4}	80	16.5	.81	8.67
42-32	56	15	4.8×10^{-6}	9.6×10^{-6}	2.8×10^{-4}	75	18.4	.81	8.84
42-36	67	65	5.5×10^{-6}	1.8×10^{-6}	9.4×10^{-5}	72	20.0	.62	9.80
42-40	60	10	2.4×10^{-5}	7.8×10^{-6}	3.0×10^{-4}	75	16.5	.8	8.72
42-46	59	20	5.4×10^{-6}	3.2×10^{-6}	1.8×10^{-4}	75	13.4	1.1	8.49
42-54	51	35	4.3×10^{-6}	5.6×10^{-6}	1.4×10^{-4}	81	25.0	1.45	6.62
42-63	58	30	4.4×10^{-6}	6.8×10^{-8}	6.8×10^{-8}	75	39.0	.58	8.43
42-64	66	55	8.4×10^{-7}	7.2×10^{-8}	2.5×10^{-5}	92	39.0	.50	6.96
42-65	60	25	4.9×10^{-6}	8.0×10^{-6}	1.0×10^{-4}	90	16.5	1.5	6.89
42-66	75	12	4.6×10^{-6}	4.4×10^{-6}	3.9×10^{-4}	91	22.0	1.5	6.76
42-67	60	30	4.4×10^{-6}	1.6×10^{-5}	1.2×10^{-4}	89	17.4	1.4	6.87
42-68	70	20	5.3×10^{-6}	5.6×10^{-6}	5.8×10^{-4}	96	36.9	1.1	6.49
42-69	50	12	6.0×10^{-6}	2.2×10^{-6}	5.2×10^{-4}	73	14.0	.79	8.79
42-71	69	61	4.8×10^{-6}	1.7×10^{-8}	2.4×10^{-5}	91	23.3	1.4	6.67

TABLE VIII (Cont.)

DIRECT CURRENT PARAMETER OF FINAL TA-2307 TRANSISTORS

Final Transistor Delivery Number 2

Unit No.	V_{CBO} 100μa Volts	V_{CEO} 100μa Volts	I_{EBO} 4V Amperes	I_{CBO} 40V Amperes	I_{CES} 40V Amperes	LV_{CER} 50ma R-10Ω	h_{FE} V_{CE}-10V I_C-350ma	V_{CE}(sat) I_C-750ma I_B-140ma	C_{OB} 40V μμf
42-72	62	50	5.8×10^{-6}	6.1×10^{-6}	5.6×10^{-5}	91	29.1	1.2	6.61
42-74	50	50	6.2×10^{-6}	2.6×10^{-9}	4.4×10^{-8}	72	17.5	1.2	6.97
42-75	60	45	4.8×10^{-6}	1.6×10^{-6}	3.6×10^{-5}	92	69.5	1.1	6.33
42-78	73	30	4.6×10^{-6}	2.3×10^{-7}	1.3×10^{-4}	101	29.2	1.3	6.34
42-81	40	12	2.4×10^{-6}	1.4×10^{-4}	4.0×10^{-4}	105	15.9	.95	-
42-82	65	40	4.8×10^{-6}	5.1×10^{-7}	9.1×10^{-5}	95	35.0	1.1	6.39
42-83	40	6.0	2.6×10^{-6}	1.1×10^{-4}	7.1×10^{-4}	82	23.3	1.0	7.53
43-2	60	60	1.4×10^{-6}	1.3×10^{-10}	1.3×10^{-10}	94	21.9	.9	6.53
43-6	71	71	1.9×10^{-6}	3.4×10^{-10}	3.4×10^{-10}	90	39.0	.8	6.7
43-7	73	73	5.0×10^{-5}	6.2×10^{-7}	1.2×10^{-5}	100	17.0	1.2	6.26
43-8	60	60	9.0×10^{-8}	7.2×10^{-11}	7.2×10^{-11}	94	14.0	.9	6.61
44-2	48	.0	4.2×10^{-6}	6.3×10^{-6}	7.6×10^{-4}	70	14.6	1.4	6.56
44-4	62	43	3.8×10^{-6}	8.4×10^{-7}	5.4×10^{-5}	83	14.6	1.8	6.24
44-5	60	60	3.6×10^{-6}	3.1×10^{-10}	3.0×10^{-10}	85	14.0	1.6	6.57
44-8	58	56	1.9×10^{-6}	1.1×10^{-8}	2.2×10^{-5}	84	14.0	1.4	6.73
44-12	69	53	7.4×10^{-6}	2.0×10^{-8}	1.9×10^{-5}	80	14.0	1.3	6.57
44-21	65	65	9.4×10^{-7}	3.2×10^{-10}	3.2×10^{-10}	80	20.0	1.2	6.36
44-26	61	61	4.1×10^{-6}	2.2×10^{-9}	4.1×10^{-6}	80	15.9	1.4	6.66
44-27	65	65	3.8×10^{-6}	5.8×10^{-9}	8.1×10^{-6}	89	11.7	2.0	6.48

TABLE VIII (Cont.)

DIRECT CURRENT PARAMETER OF FINAL TA-2307 TRANSISTORS

Final Transistor Delivery Number 2

Unit No.	V_{CBO} 100μa Volts	V_{CEO} 100μa Volts	I_{EBO} 4V Amperes	I_{CBO} 40V Amperes	I_{CES} 40V Amperes	LV_{CER} 50ma R-10Ω	h_{FE} V_{CE}-10V I_C-350ma	V_{CE}(sat) I_C-750ma I_B-140ma	C_{OB} 40V μμf
44-33	65	65	9.5×10^{-7}	1.9×10^{-10}	2.0×10^{-10}	92	19.4	1.4	6.23
44-36	67	67	9.0×10^{-6}	2.0×10^{-10}	2.0×10^{-10}	90	13.5	1.6	6.48
44-38	63	61	5.8×10^{-4}	1.2×10^{-6}	1.7×10^{-5}	90	11.7	1.8	6.47
44-41	65	64	9.2×10^{-7}	2.2×10^{-8}	2.4×10^{-5}	84	11.5	1.3	6.77
44-43	66	57	4.0×10^{-6}	9.2×10^{-8}	4.4×10^{-5}	90	14.0	1.6	6.51
44-46	75	75	9.1×10^{-7}	8.4×10^{-9}	8.6×10^{-9}	100	27.7	2.0	6.26
44-52	71	71	3.4×10^{-6}	5.9×10^{-9}	8.6×10^{-6}	100	8.8	2.0	6.45
44-53	65	60	6.6×10^{-7}	3.1×10^{-8}	4.5×10^{-5}	92	18.0	1.1	6.21
44-54	60	60	3.2×10^{-6}	1.8×10^{-10}	1.8×10^{-10}	90	8.35	2.3	6.41
44-56	75	75	5.0×10^{-6}	2.8×10^{-10}	2.8×10^{-10}	78	8.75	2.0	6.64
44-57	75	75	9.0×10^{-7}	1.8×10^{-8}	1.2×10^{-6}	90	10.0	2.0	6.55
44-58	65	65	8.0×10^{-6}	2.4×10^{-10}	2.4×10^{-6}	97	12.9	1.7	6.51
44-63	70	70	4.0×10^{-6}	7.8×10^{-9}	6.2×10^{-6}	95	11.7	1.8	6.41
44-65	48	45	3.8×10^{-6}	9.9×10^{-9}	8.6×10^{-6}	98	7.8	2.4	6.56
44-66	71	71	3.6×10^{6}	3.0×10^{-8}	1.8×10^{-5}	97	8.35	2.0	6.30
44-70	70	70	9.2×10^{-4}	7.1×10^{-7}	1.6×10^{-6}	97	12.5	2.2	6.59
44-71	62	10.0	4.9×10^{-7}	1.2×10^{-4}	3.0×10^{-4}	99	44.0	.8	6.68
44-72	65	63	9.0×10^{-7}	1.6×10^{-10}	1.4×10^{-10}	95	12.8	1.8	6.15

TABLE VIII (Cont.)

DIRECT CURRENT PARAMETER OF FINAL TA-2307 TRANSISTORS

Final Transistor Delivery Number 2

Unit No.	V_{CBO} 100μa Volts	V_{CEO} 100μa Volts	I_{EBO} 4V Amperes	I_{CBO} 40V Amperes	I_{CES} 40V Amperes	LV_{CER} 50ma R-100	h_{FE} V_{CE}-10V I_C-350ma	V_{CE}(sat) I_C-750ma I_B-140ma	C_{OB} 40V μμf
44-73	68	68	6.4×10^{-6}	2.0×10^{-10}	2.0×10^{-10}	89	8.8	2.2	6.22
44-76	65	65	5.8×10^{-7}	1.9×10^{-9}	1.2×10^{-5}	100	20.6	1.0	6.31
44-78	70	50	5.4×10^{-6}	3.2×10^{-7}	4.8×10^{-5}	96	17.5	1.8	6.38
44-79	68	65	5.4×10^{-6}	1.4×10^{-6}	5.2×10^{-5}	90	14.0	1.9	6.69
44-80	78	30	4.4×10^{-6}	6.5×10^{-7}	1.0×10^{-9}	118	25.0	1.9	5.75
44-81	72	72	4.6×10^{-6}	4.8×10^{-8}	2.8×10^{-5}	105	14.5	1.8	5.84
44-82	69	61	5.1×10^{-6}	9.8×10^{-9}	2.2×10^{-6}	100	11.6	2.2	6.31
44-84	66	40	5.0×10^{-6}	2.1×10^{-6}	8.0×10^{-5}	95	17.5	2.0	6.25
44-85	71	71	5.5×10^{-6}	1.3×10^{-10}	1.3×10^{-10}	95	9.2	2.0	6.02
44-86	65	65	4.8×10^{-6}	8.8×10^{-10}	1.3×10^{-8}	85	13.0	1.9	6.62
44-87A	75	75	3.0×10^{-4}	1.5×10^{-6}	3.4×10^{-6}	105	18.4	2.0	6.2
44-87	68	68	4.7×10^{-6}	9.8×10^{-11}	1.2×10^{-10}	100	23.2	2.4	5.84
44-93	68	60	4.8×10^{-6}	1.4×10^{-9}	4.0×10^{-7}	100	19.5	2.0	6.3
44-94	71	71	6.6×10^{-6}	1.4×10^{-10}	1.4×10^{-10}	81	10.0	2.0	6.3
44-95	66	63	5.7×10^{-6}	3.4×10^{-8}	1.8×10^{-5}	80	13.5	2.3	6.5
44-96	72	65	4.5×10^{-6}	1.6×10^{-7}	4.4×10^{-5}	100	15.9	2.1	5.8
44-97	73	35	4.2×10^{-6}	1.5×10^{-7}	9.3×10^{-5}	90	11.6	1.9	6.5
44-98	70	70	5.2×10^{-6}	1.5×10^{-7}	3.1×10^{-5}	100	9.5	2.5	-
44-100	60	58	2.8×10^{-6}	3.4×10^{-8}	3.8×10^{-5}	89	11.6	2.1	6.29

TABLE VIII (Cont.)

DIRECT CURRENT PARAMETER OF FINAL TA-2307 TRANSISTORS

Final Transistor Delivery Number 2

Unit No.	V_{CBO} 100μa Volts	V_{CEO} 100μa Volts	I_{EBO} 4V Amperes	I_{CBO} 40V Amperes	I_{CES} 40V Amperes	LV_{CER} 50ma R-10Ω	h_{FE} V_{CE}-10V I_C-350ma	V_{CE}(sat) I_C-750ma I_B-140ma	C_{OB} 40V μμf
44-104	70	69	4.8×10^{-6}	5.2×10^{-8}	1.6×10^{-5}	83	13.4	2.4	6.67
44-105	70	70	5.2×10^{-6}	1.5×10^{-10}	1.5×10^{-10}	90	14.0	2.6	6.44
44-108	62	62	6.2×10^{-4}	1.6×10^{-7}	1.5×10^{-6}	80	7.8	1.5	6.26
44-109	64	64	9.1×10^{-7}	1.8×10^{-9}	1.8×10^{-9}	70	17.5	2.3	6.0
44-110	75	75	4.4×10^{-6}	4.0×10^{-10}	4.0×10^{-10}	92	19.4	1.95	6.22
44-104	62	62	7.0×10^{-6}	2.0×10^{-6}	2.0×10^{-6}	79	10.0	2.3	6.7
44-113	72	72	5.5×10^{-6}	4.4×10^{-10}	7.1×10^{-9}	90	18.4	2.1	7.79
44-114	61	60	$.4 \times 10^{-6}$	3.0×10^{-10}	4.4×10^{-6}	85	8.75	.9	6.48
44-116	65	62	4.3×10^{-6}	2.0×10^{-8}	1.2×10^{-5}	70	8.5	2.3	6.10
44-118	73	50	4.2×10^{-6}	2.6×10^{-8}	5.7×10^{-5}	80	12.0	2.4	5.42
44-121	71	3.5	7.2×10^{-6}	7.0×10^{-6}	2.6×10^{-4}	80	13.4	2.6	5.39
44-123	76	14	4.4×10^{-6}	7.0×10^{-6}	2.6×10^{-4}	100	14.0	1.8	5.95
44-124	70	70	4.1×10^{-11}	6.0×10^{-10}	2.4×10^{-6}	72	11.3	2.0	6.55
44-127	28	20	4.2×10^{-6}	2.3×10^{-4}	2.3×10^{-4}	69	25.0	1.6	6.14
44-131	69	68	4.8×10^{-6}	1.2×10^{-10}	1.2×10^{-10}	73	14.6	1.95	6.53
44-134	68	68	4.6×10^{-6}	1.4×10^{-6}	1.4×10^{-6}	70	9.0	2.1	6.31
44-136	59	59	6.0×10^{-6}	2.4×10^{-10}	2.4×10^{-10}	80	10.6	2.0	6.61
44-137	77	75	4.8×10^{-6}	3.0×10^{-8}	2.0×10^{-5}	105	11.7	2.3	5.79
44-138	69	68	4.1×10^{-6}	3.4×10^{-10}	3.4×10^{-10}	100	9.2	2.3	6.76

TABLE VIII (Cont.)

DIRECT CURRENT PARAMETER OF FINAL TA-2307 TRANSISTORS

Final Transistor Delivery Number 2

Unit No.	V_{CBO} 100μa Volts	V_{CEO} 100μa Volts	I_{EBO} 4V Amperes	I_{CBO} 40V Amperes	I_{CES} 40V Amperes	LV_{CER} 50ma R-10Ω	h_{FE} V_{CE}-10V I_C-350ma	V_{CE}(sat) I_C-750ma I_B-140ma	C_{OB} 40V μμf
44-139	70	70	4.2×10^{-6}	3.3×10^{-8}	4.2×10^{-6}	100	14.0	2.0	6.03
44-140	59	59	4.4×10^{-6}	1.8×10^{-8}	1.4×10^{-5}	82	8.55	2.0	5.35
44-141	70	30	4.5×10^{-6}	1.2×10^{-6}	1.2×10^{-6}	90	14.0	2.1	4.93
44-147	70	70	4.5×10^{-6}	1.6×10^{-10}	1.6×10^{-10}	91	10.9	1.2	6.81
44-148	73	72	2.2×10^{-6}	5.0×10^{-8}	2.4×10^{-5}	80	20.3	1.8	2.53
44-151	72	43	5.6×10^{-6}	5.2×10^{-8}	5.6×10^{-5}	87	25.0	1.6	6.20
44-152	62	62	4.6×10^{-6}	3.6×10^{-9}	2.6×10^{-6}	72	9.2	3.0	6.20
44-154	63	62	4.6×10^{-6}	1.6×10^{-10}	1.6×10^{-10}	81	12.9	2.0	6.68
44-159	62	61	3.4×10^{-6}	4.9×10^{-10}	4.9×10^{-10}	98	15.9	1.6	6.72
44-160	73	73	7.2×10^{-6}	5.0×10^{-10}	4.5×10^{-10}	100	21.8	1.0	6.57
44-167	58	58	1.0×10^{-6}	1.1×10^{-9}	1.1×10^{-9}	71	26.9	1.1	7.00
44-168	60	60	3.0×10^{-4}	9.6×10^{-10}	1.1×10^{-9}	88	22.3	1.1	6.82
44-169	69	68	1.2×10^{-6}	7.0×10^{-7}	6.8×10^{-7}	90	39.0	.95	6.86
44-170	70	70	7.0×10^{-6}	7.8×10^{-10}	8.0×10^{-10}	100	14.6	1.2	6.75
44-171	76	69	5.0×10^{-6}	1.8×10^{-7}	6.2×10^{-6}	103	70.0	.8	6.40
44-172	76	70	$.5 \times 10^{-6}$	1.9×10^{-9}	1.9×10^{-9}	100	70.0	.9	7.44
44-174	70	69	3.0×10^{-6}	6.6×10^{-10}	6.6×10^{-10}	91	15.2	1.1	7.06
44-175	75	60	7.6×10^{-8}	2.0×10^{-9}	2.0×10^{-9}	100	50.0	.9	6.77
44-180	70	60	9.1×10^{-8}	5.2×10^{-10}	5.2×10^{-10}	98	44.0	1.1	6.79

TABLE VIII (Cont.)

DIRECT CURRENT PARAMETER OF FINAL TA-2307 TRANSISTOR

Final Transistor Delivery Number 2

Unit No.	V_{CBO} 100μa Volts	V_{CEO} 100μa Volts	I_{EBO} 4V Amperes	I_{CBO} 40V Amperes	I_{CES} 40V Amperes	LV_{CER} 50ma R-100	h_{FE} V_{CE}-10V I_C-350ma	V_{CE}(sat) I_C-750ma I_B-140ma	C_{OB} 40V μμf
44-181	70	60	9.2×10^{-8}	1.9×10^{-9}	1.9×10^{-9}	93	44.0	1.1	6.79
44-182	38	35	5.8×10^{-7}	2.6×10^{-10}	2.8×10^{-10}	86	41.0	1.05	6.81
44-183	70	65	9.8×10^{-10}	3.8×10^{-10}	3.8×10^{-10}	90	31.8	1.1	7.04
44-184	70	69	8.2×10^{-7}	4.6×10^{-4}	4.6×10^{-4}	100	13.5	1.4	-
44-186	72	72	6.0×10^{-6}	7.4×10^{-10}	7.4×10^{-10}	90	13.0	1.5	6.78
44-187	70	70	3.8×10^{-6}	3.7×10^{-10}	3.7×10^{-10}	90	50.0	1.1	7.44
44-190	65	21	7.9×10^{-8}	4.8×10^{-5}	3.6×10^{-4}	100	63.2	.9	6.81
44-193	68	65	1.6×10^{-6}	3.6×10^{-8}	4.2×10^{-5}	82	21.9	1.1	6.70
44-196	71	70	2.7×10^{-6}	4.9×10^{-9}	4.9×10^{-9}	95	58.0	1.9	7.08
44-199	55	19	6.0×10^{-7}	6.6×10^{-7}	2.6×10^{-4}	65	20.0	1.8	6.22
44-202	55	40	7.4×10^{-8}	4.8×10^{-5}	1.2×10^{-4}	78	11.7	1.35	6.55
44-204	56	23	2.7×10^{-4}	5.2×10^{-5}	2.4×10^{-4}	65	17.7	4.0	6.05
44-206	60	60	5.7×10^{-7}	1.6×10^{-5}	3.2×10^{-6}	69	15.9	2.0	6.39
44-209	55	14	6.4×10^{-7}	6.0×10^{-6}	2.6×10^{-4}	70	44.0	1.65	6.09
44-211	62	62	2.0×10^{-6}	1.1×10^{-9}	1.1×10^{-9}	80	17.5	1.8	6.25
44-213	62	62	2.3×10^{-6}	1.2×10^{-9}	1.2×10^{-9}	80	17.5	1.7	6.41
44-214	53	48	$.5 \times 10^{-6}$	3.6×10^{-7}	3.6×10^{-7}	80	11.7	1.2	6.54
44-215	66	50	7.4×10^{-8}	5.4×10^{-10}	2.4×10^{-9}	81	87.5	1.8	6.70
44-218	57	57	7.0×10^{-7}	6.8×10^{-9}	8.6×10^{-6}	68	23.3	2.5	5.98

TABLE VIII (Cont.)

DIRECT CURRENT PARAMETER OF FINAL TA-2307 TRANSISTOR

Final Transistor Delivery Number 2

Unit No.	V_{CBO} 100μa Volts	V_{CEO} 100μa Volts	I_{EBO} 4V Amperes	I_{CBO} 40V Amperes	I_{CES} 40V Amperes	LV_{CER} 50ma R-10Ω	h_{FE} V_{CE}-10V I_C-350ma	V_{CE}(sat) I_C-750ma I_B-140ma	C_{OB} 40V μμf
44-219	62	29	2.6×10^{-6}	6.0×10^{-7}	1.4×10^{-4}	71	16.7	2.1	6.32
44-225	59	52	9.1×10^{-8}	9.4×10^{-7}	2.7×10^{-5}	72	46.6	1.3	6.39
44-230	48	48	3.6×10^{-6}	4.0×10^{-5}	4.0×10^{-5}	78	20.3	2.5	-
44-231	68	62	$.8 \times 10^{-6}$	7.0×10^{-10}	7.0×10^{-10}	91	39.9	1.7	6.22
44-232	65	65	8.0×10^{-8}	9.0×10^{-10}	9.0×10^{-10}	72	39.0	1.9	6.24
44-252	53	25	6.2×10^{-7}	6.4×10^{-5}	2.0×10^{-4}	92	26.0	1.9	7.48
45-1	72	60	5.1×10^{-6}	2.5×10^{-8}	2.9×10^{-5}	82	23.4	1.75	6.6
45-2	65	50	6.6×10^{-4}	5.2×10^{-6}	1.9×10^{-5}	100	39.0	1.6	5.3
45-3	62	62	4.5×10^{-6}	7.0×10^{-9}	7.1×10^{-6}	81	15.0	1.6	6.4
45-6	62	16	4.2×10^{-6}	1.4×10^{-6}	2.5×10^{-4}	98	19.0	1.2	6.1
45-8	38	2.8	4.0×10^{-8}	1.2×10^{-4}	6.6×10^{-4}	89	17.0	1.6	6.7
45-9	60	35	4.0×10^{-6}	2.9×10^{-7}	8.6×10^{-5}	83	14.0	1.5	6.3
45-10	78	9.0	4.7×10^{-6}	1.8×10^{-6}	8.6×10^{-4}	80	17.0	1.2	6.3
45-12	70	21	9.0×10^{-7}	5.2×10^{-7}	1.8×10^{-4}	100	19.0	1.0	6.0
45-13	80	14	3.8×10^{-6}	2.2×10^{-7}	3.5×10^{-4}	100	14.0	1.8	6.2
45-14	85	20	4.4×10^{-6}	8.8×10^{-7}	8.0×10^{-4}	100	17.5	2.3	6.11
45-17	71	36	9.0×10^{-7}	3.8×10^{-7}	8.0×10^{-5}	90	20.0	1.5	6.5
45-20	79	79	5.2×10^{-4}	6.3×10^{-6}	8.6×10^{-6}	95	14.0	1.6	6.4
45-21	72	72	3.6×10^{-6}	5.0×10^{-11}	5.0×10^{-11}	94	14.0	1.8	6.46

TABLE VIII (Cont.)

DIRECT CURRENT PARAMETER OF FINAL TA-2307 TRANSISTOR

Final Transistor Delivery Number 2

Unit No.	V_{CBO} 100μa Volts	V_{CEO} 100μa Volts	I_{EBO} 4V Amperes	I_{CBO} 40V Amperes	I_{CES} 40V Amperes	LV_{CER} 50ma R-100Ω	h_{FE} V_{CE}-10V I_C-350ma	$V_{CE}(sat)$ I_C-750ma I_B-140ma	C_{OB} 40V μμf
45-22	70	9.0	4.4×10^{-6}	9.8×10^{-7}	5.6×10^{-4}	95	23.0	1.6	5.9
45-23	70	70	4.0×10^{-4}	2.6×10^{-10}	2.6×10^{-10}	82	16.0	1.6	6.8
45-26	75	65	8.6×10^{-7}	2.2×10^{-8}	1.9×10^{-5}	95	15.0	1.8	7.3
45-29	75	42	9.5×10^{-7}	1.8×10^{-7}	6.0×10^{-5}	71	21.0	1.8	6.22
45-30	33	6.0	4.1×10^{-6}	1.2×10^{-4}	3.6×10^{-4}	76	14.0	1.4	6.1
45-34	68	30	3.6×10^{-6}	1.6×10^{-6}	1.2×10^{-4}	90	19.0	1.6	6.38
45-35	68	68	9.0×10^{-7}	1.8×10^{-10}	1.8×10^{-10}	95	14.0	1.5	6.3
45-36	70	12	4.6×10^{-6}	4.0×10^{-6}	4.0×10^{-4}	95	25.0	1.6	6.1
45-39	50	10	8.5×10^{-7}	5.0×10^{-5}	9.2×10^{-4}	100	29.0	1.6	5.7
45-41	80	13	4.0×10^{-6}	5.8×10^{-7}	3.9×10^{-4}	98	14.0	1.9	6.0

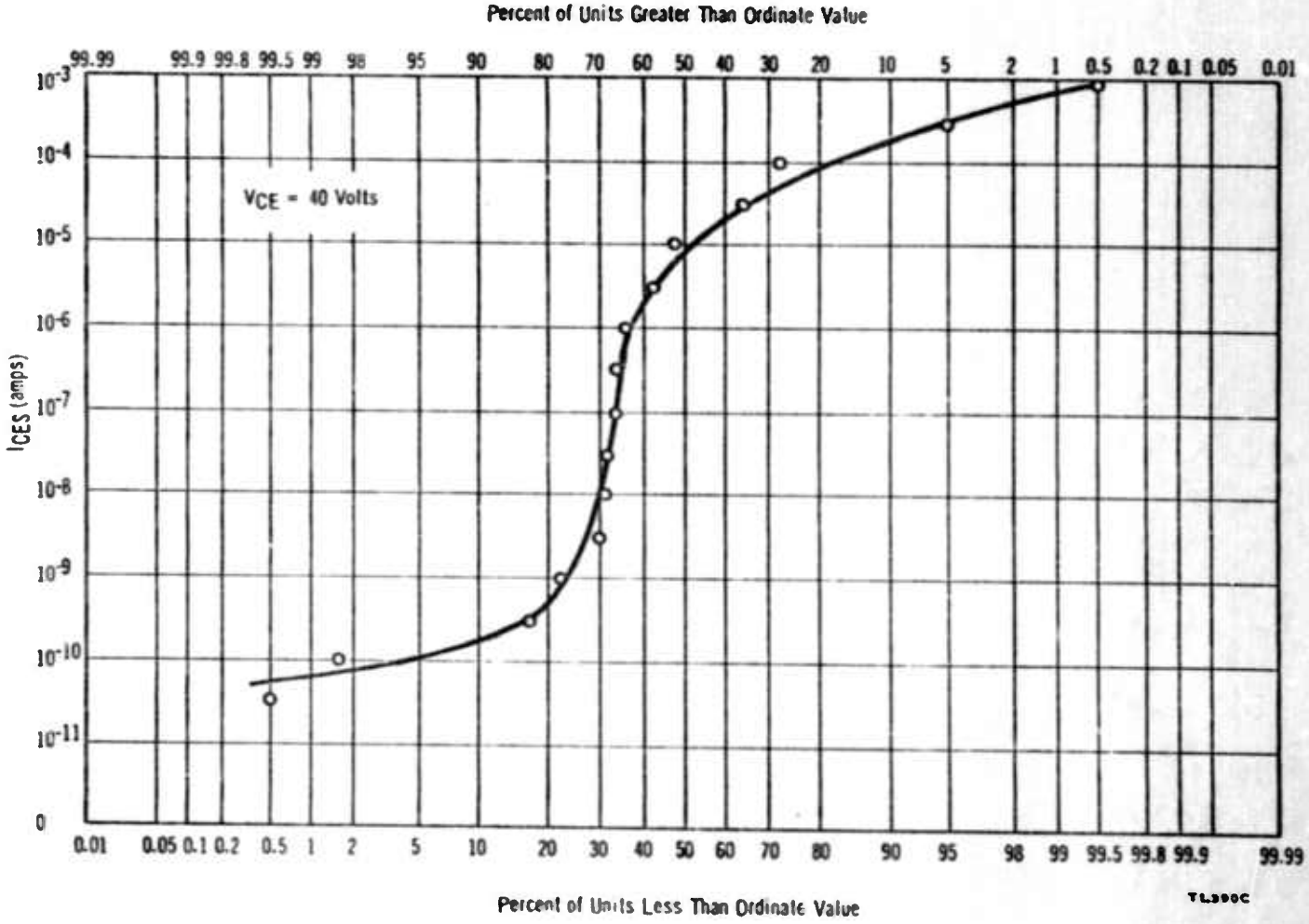


FIGURE 26 DISTRIBUTION OF COLLECTOR CUTOFF CURRENT (I_{CES}) OF FINAL TA2307 TRANSISTORS

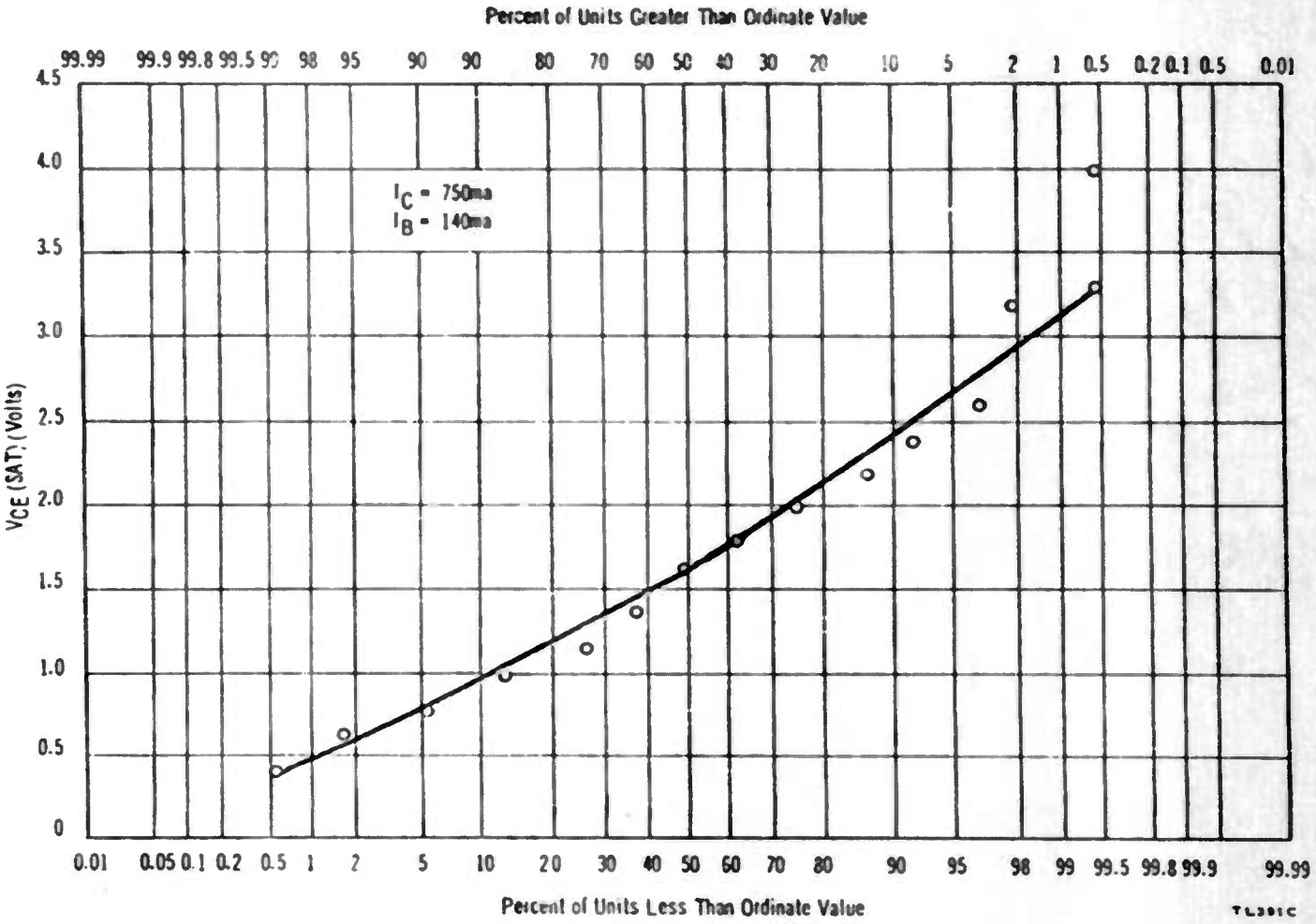


FIGURE 27 DISTRIBUTION OF COLLECTOR SATURATION VOLTAGE, V_{CE} (SAT), OF FINAL TA2307 TRANSISTORS

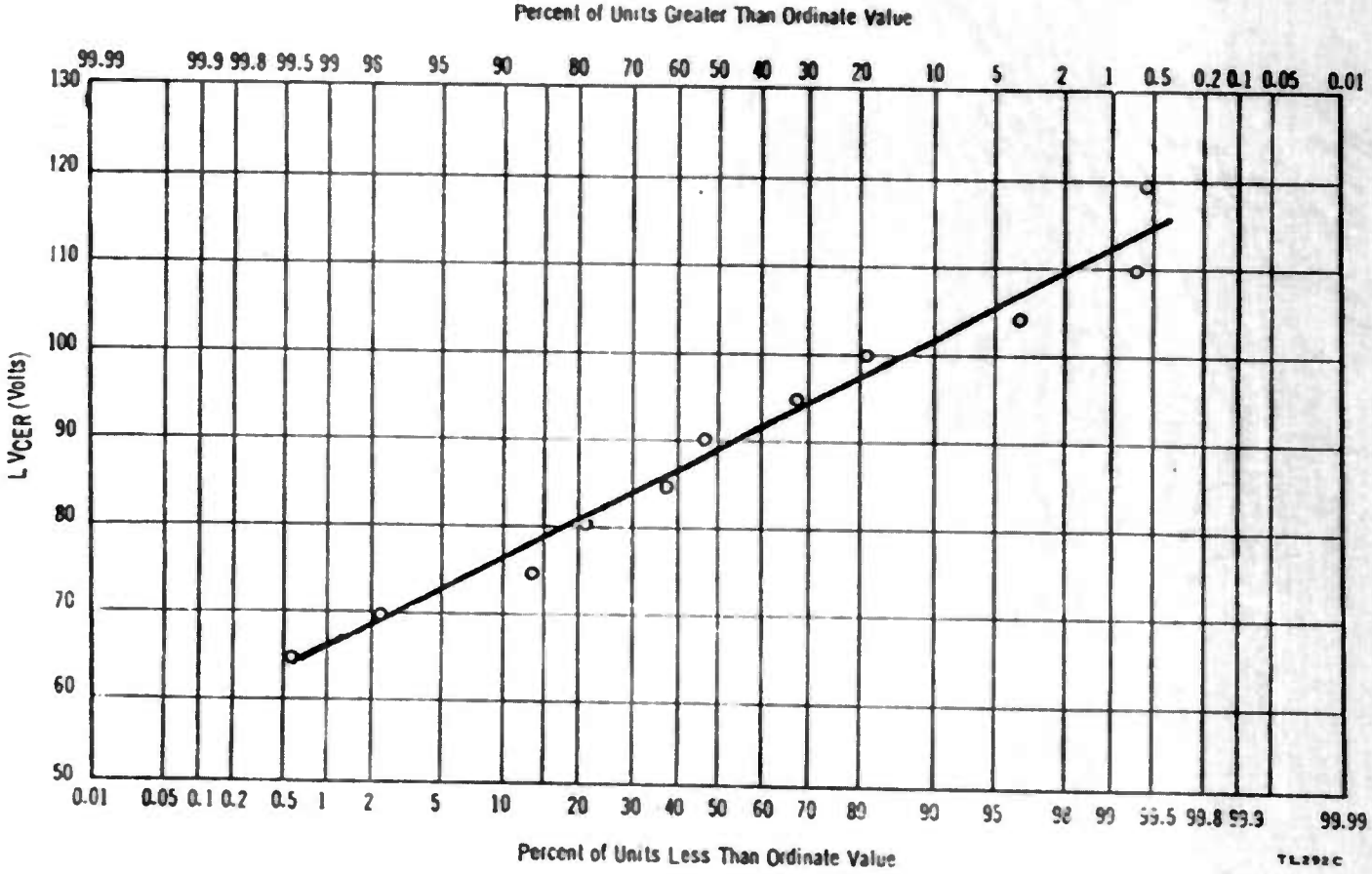


FIGURE 28 DISTRIBUTION OF SUSTAINING VOLTAGE ($L V_{CER}$) OF FINAL TA2307 TRANSISTORS

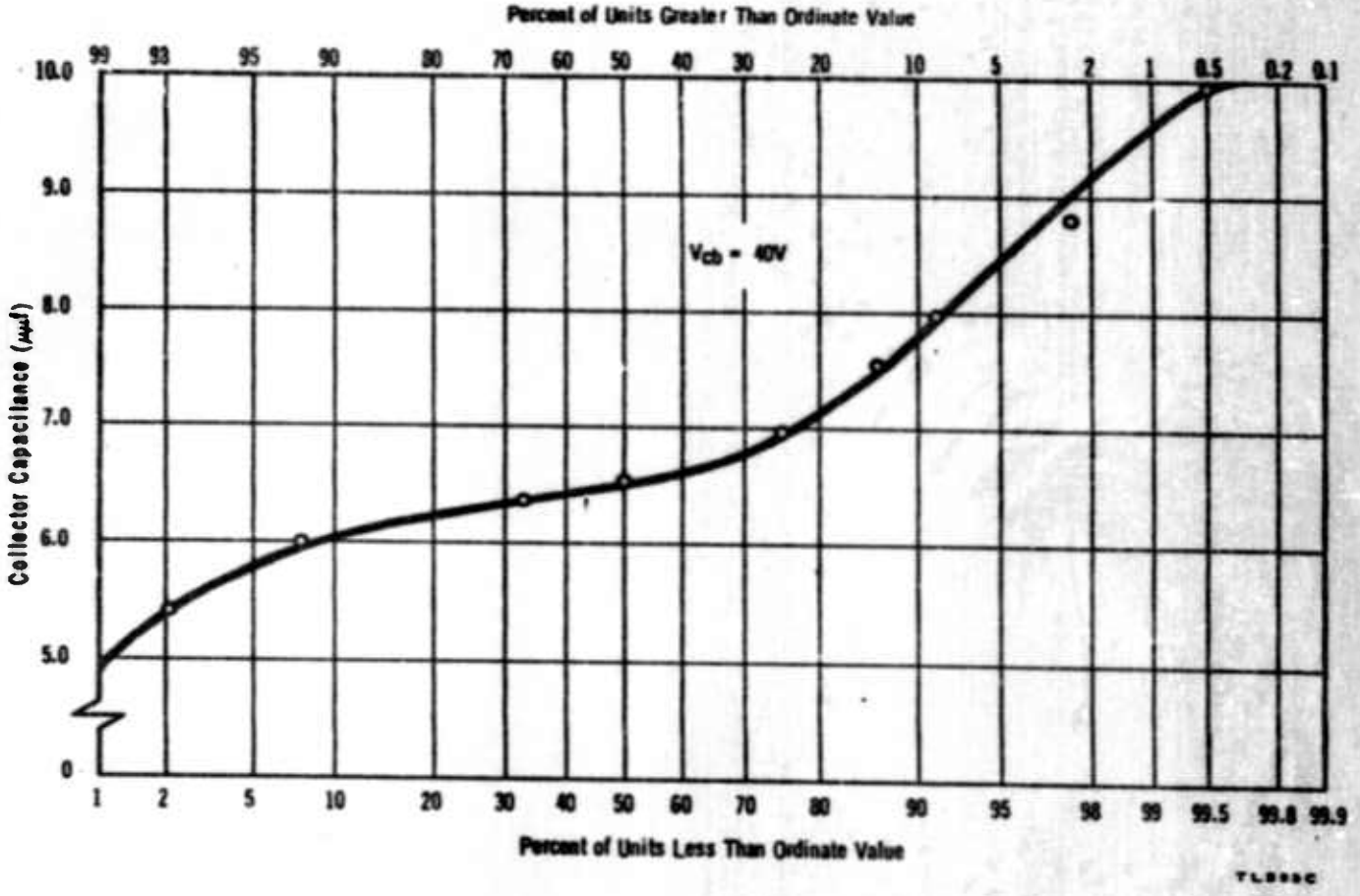


FIGURE 29 DISTRIBUTION OF COLLECTOR CAPACITANCE, C_{ob} OF FINAL TA-2307 TRANSISTORS

on a Boonton Type Model 75A-S8 Capacitance Bridge. Capacitance effects associated with the device socket are nulled out of the equipment prior to measurement of the devices. The accuracy of the capacitance bridge is ±3 percent. A precision voltmeter having an accuracy of one percent is used to monitor the collector voltage.

The emitter cutoff current (I_{EBO}) at 4.0 volts reverse bias between emitter and base and the collector-base leakage current (I_{CBO}) at 40 volts reverse bias between collector and base given in Table VIII are measured in the same equipment as the collector cutoff current (I_{CES}).

The collector base breakdown voltage (V_{CBO}) and the collector emitter breakdown voltage (V_{CEO}) at 100 microamperes are measured using a calibrated Tektronix Curve Tracer. This data is presented in the table.

The static forward current transfer ratio (h_{FE}) is measured at a collector potential of 10 volts and a collector current of 350 milliamperes using the Tektronix Curve Tracer. The measurements of this parameter on the final samples are shown in the table.

2. Radio Frequency Parameters

a. Measurement of $r_{bb'}$

The base lead resistance was measured on a General Radio bridge. The input impedance h_{ie} was measured as a function of frequency.

The results were plotted on a Smith Chart and the point where the curve intersected the real axis, showing zero reactance, was taken as $r_{bb'}$. This occurred at about 200 mc where subsequent units were measured. Sample measurements of $r_{bb'}$ on the final transistors are shown in Table IX.

b. Measurement of f_T

Gain-bandwidth (f_T) is determined by measuring h_{fe} at a frequency where h_{fe} is decreasing at 6db/octave and using the equation:

$$f_T = h_{fe} \times f \text{ measurement.}$$

Devices were sampled for f_T measurements at a collector voltage of 10 volts, a collector current of 200 milliamperes and a frequency of 500 megacycles. The measured values are presented in Table IX. The measurement was made on a GR-1607-A transfer function and emittance bridge.

3. Mechanical and Environmental

Ten finished transistors were subjected to Group B inspection. The tests included in this inspection were:

1. Moisture Resistance (helium leak test)
2. Vibration (variable frequency)
3. Shock (non-operating, 500g)
4. Constant Acceleration (10,000g)
5. Temperature Cycling (-65°C to 200°C 5 cycles)

TABLE IX

SAMPLE MEASUREMENTS OF BASE SPREADING RESISTANCE, r_{bb}' AND GAIN BANDWIDTH PRODUCT, f_t

Unit No.	f_t V_{CE}= 10V I_C= 200ma f= 500mc	r_{bb}' V_{CE}= 10V I_C= 200ma f= 500mc
37-27	332	-
34-13	398	-
41-34	550	-
34-19	400	-
37-30	464	-
37-33	580	-
34-18	390	-
37-5	520	-
37-7	604	-
41-33	528	-
37-9	588	-
41-32	532	-
41-27	436	-
34-9	520	-
31-3	270	-
37-23	432	-
34-1	380	-
26-31	158	-
30-20	266	-
34-42	448	-
40-14	605	-
40-28	540	-
41-10	-	11.6
41-53	-	12.0
41-67	725	13.5
41-76	725	12.4
42-67	700	12.5

Unit No.	f_t V_{CE}= 10V I_C= 200ma f= 500mc	r_{bb}' V_{CE}= 10V I_C= 200ma f=250 mc
42-68	755	-
42-69	700	10.6
42-72	730	12.0
44-87	720	-
44-105	690	-
44-110	695	-
44-113	750	-
44-127	680	-
44-137	685	12.4
44-138	650	12.0
44-151	770	-
44-152	685	-
44-168	590	10.1
44-170	560	10.3
44-182	625	11.6
44-184	665	12.3
44-186	585	-
44-187	680	-
44-199	725	-
44-202	705	-
44-204	670	-
44-206	635	-
44-209	770	-
44-252	675	-
45-1	715	-
45-2	725	-
45-14	730	-

6. Vibration (fatigue)

7. Storage Life (200°C, 1000 hours)

The collector cutoff current (I_{CEO} and I_{CES}) at a collector voltage of 28 volts and the emitter cutoff current (I_{EBO}) at an emitter voltage of 4 volts were measured after each test.

Two of the ten units indicated leaks during the helium leak test. No failures occurred during vibration (variable frequency), shock (500g) or vibration (fatigue) tests.

Two failures occurred during the constant acceleration test. One unit showed an emitter-base short and another showed an emitter base and collector emitter open. Examination of these units revealed that a portion of the gold metallizing, containing the bonded emitter wires, had pulled loose from the BeO on the open unit. It was observed on the shorted unit that the first bond on the emitter bonding area was set too far back from the end of the wire. Consequently, the extended end of the emitter lead pivoted about the bond and fell across the base metallizing resulting in an emitter base short.

One failure occurred during temperature cycling while no failures were encountered in the 200°C storage life test after over 1750 hours.

Improved control on the welding cycle in the sealing operation has eliminated helium leak test failures. Over 100 sealed units have

been made with no failures.

The failure caused by the pivoting of the emitter lead across the base metallizing was eliminated by placing the first emitter bond immediately next to the end of the emitter lead.

4. Thermal Resistance

The package used in the fabrication of the final device was a 7/16" isolated collector, double ended stud. A photograph of this package is shown in Figure 30.

The berrylium oxide isolating material has a metallized tab approximately 110 mils wide and 185 mils long. Drawings of this package are shown in Figures 31, 32, and 33.

Gold-silicon was used as the alloying material between the silicon pellet and metallized ceramic. Mounting is performed at the lowest compatible temperature with the silicon pellet by the alloying material. A temperature of 450°C and a mounting atmosphere of nitrogen results in satisfactory wetting of the silicon with no degradation of the units during this operation.

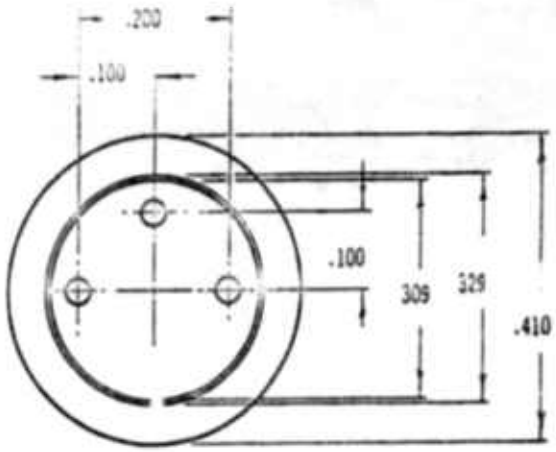
The thermal resistance is affected by the completeness of alloying obtained during mounting. Thermal resistance measurements are performed using the test set shown in Figure 34, using a common base configuration. In these measurements, the input characteristics (V_{BE}, I_B), which are a function of temperature, is determined by heating the unit under test with circulating hot water. The device

a. Front View

c. Top View

b. Side View

FIGURE 30 HIGH FREQUENCY POWER TRANSISTOR CASE (DOUBLE ENDED STUD-ISOLATED COLLECTOR)



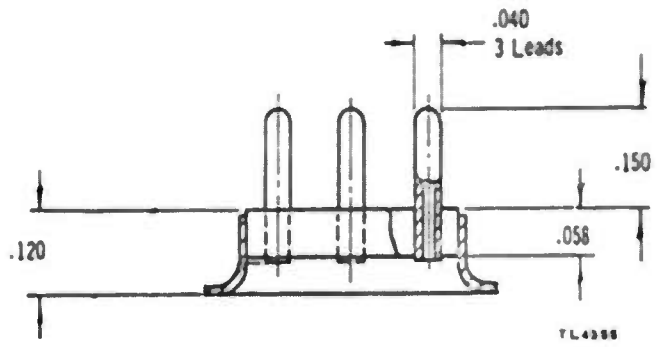


FIGURE 31 SHELL ASSEMBLY

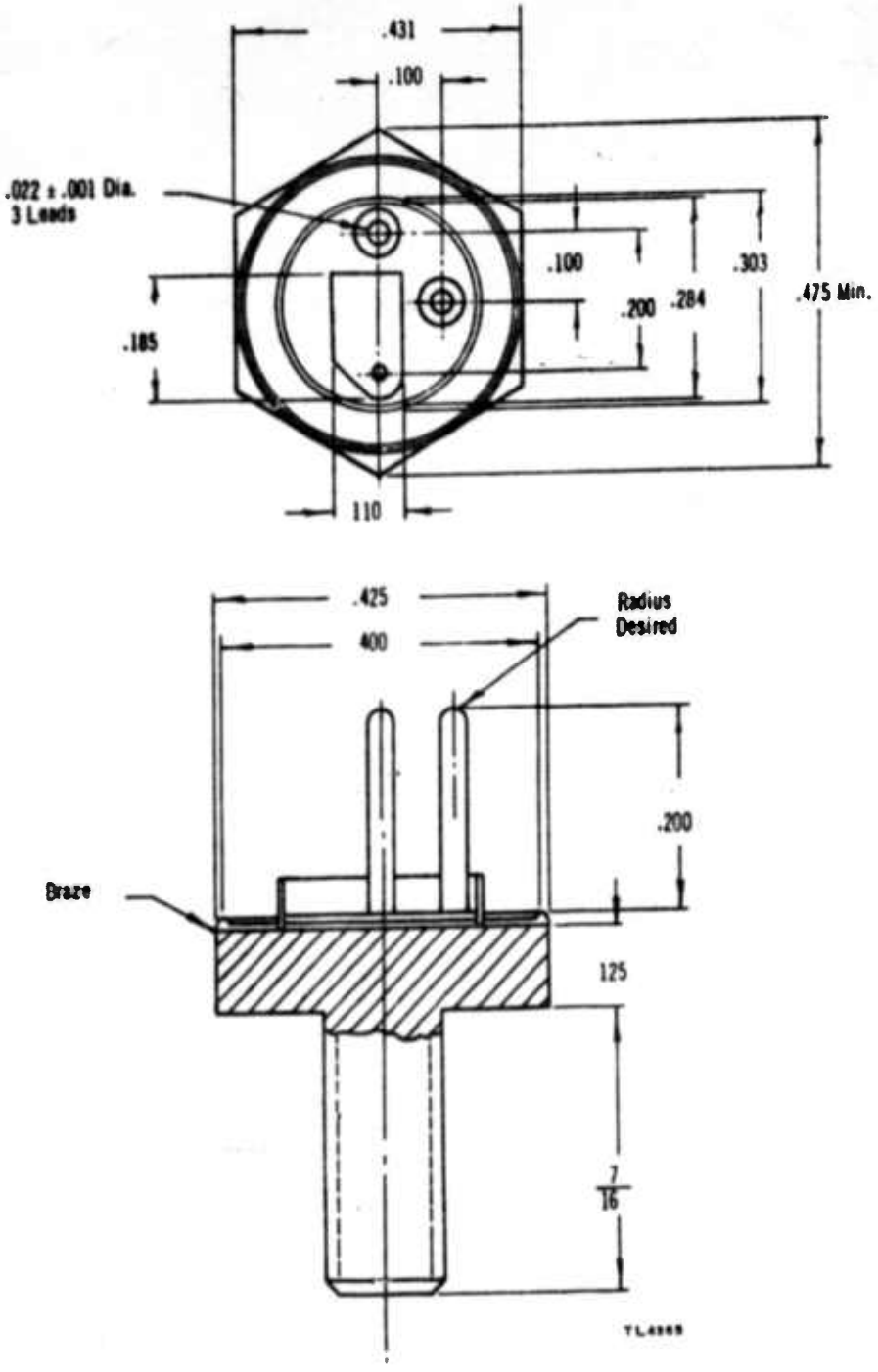


FIGURE 32 HEADER ASSEMBLY ISOLATED COLLECTOR

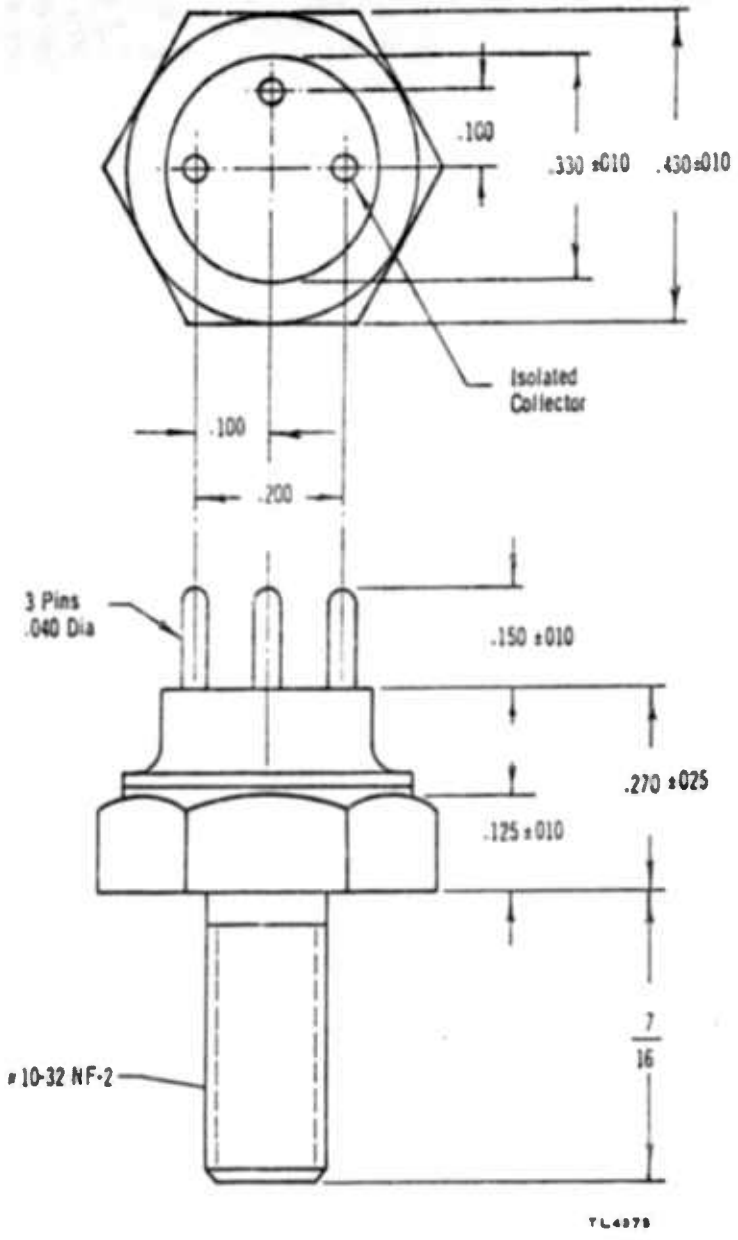


FIGURE 33 7/16 HEX ISOLATED COLLECTOR

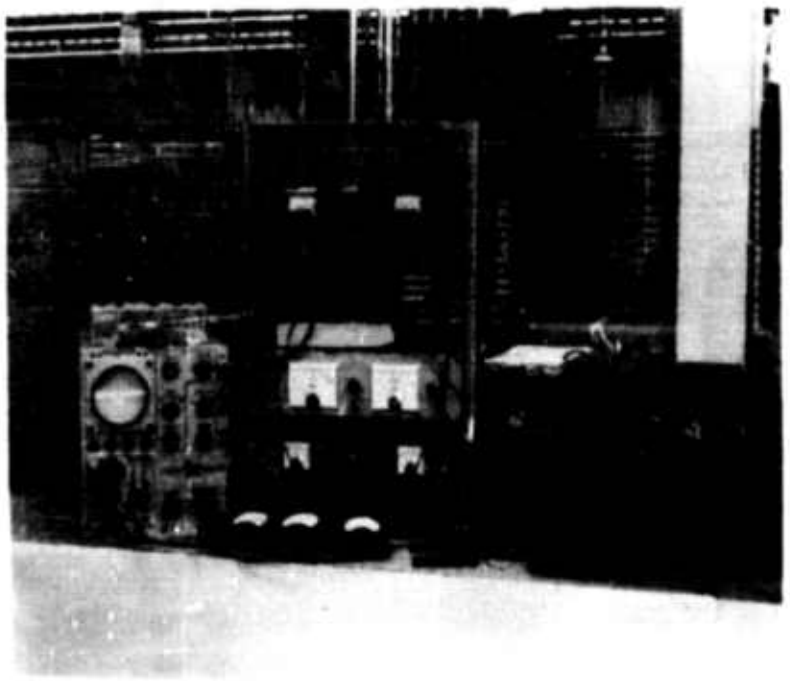


FIGURE 34 THERMAL RESISTANCE TEST SET

is monitored by a thermocouple and brought to a temperature of approximately 70° to 80°C. A short duration (2 percent duty cycle) current pulse (I_B) is then applied to the device and the input voltage (V_{BE}) is recorded. The unit is allowed to cool and then heated again by power dissipated in the device. The same amplitude base current pulse, but longer duration (98 percent duty cycle), is applied. The collector voltage is varied such that the temperature rise, due to power dissipated in the unit, results in the same V_{BE} indicating the unit is then at the same temperature as when heated with the hot water.

As previously discussed, the thermal resistance is calculated from the relationship:

$$TR = \frac{\Delta T}{P_{diss}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (18)$$

Measurements of thermal resistance on devices fabricated with the final transistors are presented in Table X. Of the 15 units measured, five had thermal resistance values greater than 14.6°C per watt.

The fifteen devices were subjected to operating life tests with conditions of 140°C case temperature and collector power dissipation of four watts at 28 volts. Of the devices tested, unit number 44-14 failed within 250 hours and unit numbers 41-18, 43-4 and 44-216 failed between 250 and 500 hours. A comparison of the life test results to the thermal resistance data shows that the units which failed also exhibited excessively high thermal resistance values.

TABLE X
THERMAL RESISTANCE MEASUREMENTS
TA-2307 TRANSISTORS

Unit No.	Thermal Resistance °C/Watt
31-24	8.5
34-39	8.7
35-17	14.0
40-20	11.0
40-35	13.0
41-18	21.0
43-4	37.0
44-14	32.0
44-123	8.9
44-166	12.2
44-179	9.2
44-201	7.5
44-216	28.0
44-217	25.0
44-223	10.7

Examination of open circuited devices during life testing showed the formation of purple plague on the emitter bonding area causing the bonding wire to be consumed in the eutectic formed.

Further studies of the thermal resistance resulted in the use of a gold and molybdenum buffer between the metallized ceramic and the silicon pellet. The molybdenum was mounted to the metallized ceramic using gold alloy preforms and the silicon pellet was mounted to the moly using the gold silicon eutectic. This mounting approach resulted in the isolation of the silicon pellet from contact with the nickel plating and subsequent materials in the ceramic metallizing.

Measurement of units mounted by this method indicated consistent thermal resistance values between 8.3 and 9.4°C/watt.

5. High Frequency Power Gain Measurements

Various high frequency test circuits were designed and constructed to evaluate the devices at ultrahigh frequencies. Initial experimental model transistors were measured in a 400 megacycle Class C common emitter amplifier shown in Figure 35.

Tuned line (distributed parameter) and lumped constant 500 megacycle circuits were fabricated in both common base and common emitter configurations. In general, considerably higher output powers were obtained in the common base chassis, however, the circuit was only conditionally stable. At 500 megacycles, the common base circuit could be tuned for maximum output power by use of the base circuit

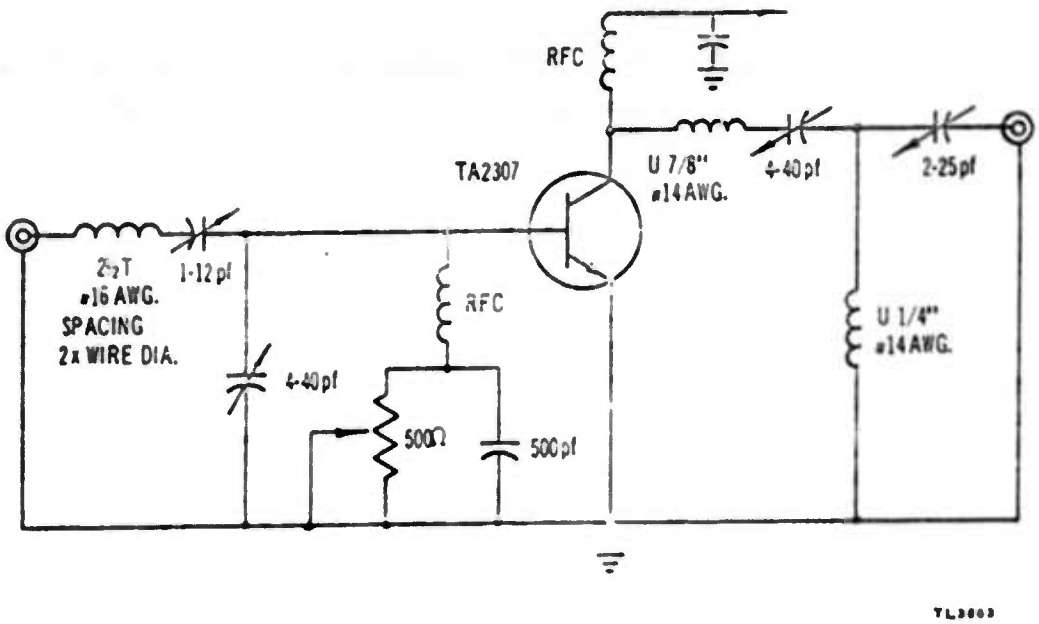


FIGURE 35 400 MEGACYCLE CLASS C COMMON EMITTER AMPLIFIER (LUMPED CONSTANT)

and collector circuit adjustable stubs. An impedance match between the device input and the signal source and between the load and the collector was obtained as indicated by an inline wattmeter. This meter measures both the power delivered to the input of the device and the power reflected back to the signal generator. The condition of zero reflected power indicates an impedance match between the signal generator and the amplifier circuit. In the common base circuit, this impedance match was obtained. However, disconnecting the signal generator resulted in oscillation of the circuit. Typical power gain data obtained on a unit in the common base circuit and in the common emitter circuit is shown in Table XI. Because of this instability exhibited by the common base circuit, it was decided that a more accurate evaluation of the device could be made in the common emitter configuration.

The finalized circuit used to evaluate the devices was an unneutralized, Class C, common emitter amplifier employing tuned lines. The use of tuned lines enabled the circuit to be applicable over a wide range of impedance matching conditions. The circuit diagram is illustrated in Figure 36 and a photograph of the circuit and associated equipment can be seen in Figure 37.

The output power obtained on the second and third group of state-of-the-art transistors in a high frequency lumped constant circuit is given in Table XII. Table XIII shows 400 megacycle data on two devices in a lumped constant and tuned line circuit. A comparison

of the units indicate the tuned line circuit results in slightly higher output power and improved efficiency. A plot of UHF output versus input power at 400 megacycles for collector voltages of 28, 40 and 50 volts is shown in Figure 38.

These state-of-the-art samples were fabricated using high resistivity starting material, deep diffusions and a medium sheet resistance of the P^+ matrix. A comparison of these units to devices fabricated on low resistivity material, using shallow diffusions and a very low P^+ layer sheet resistance, indicates the advantage associated with lower resistivity material.

Ultrahigh frequency power gain measurement data on the final samples using the circuit of Figure 36 is shown in Table XIV. These samples were fabricated using the 3-4 ohm cm starting material.

Figures 39 and 40 present distributions of the power output and circuit efficiency of the final samples.

A plot of power output versus frequency for an input signal level of one watt at collector potentials of 40 and 50 volts is depicted in Figure 41. No data was obtained beyond the 750 megacycle point shown on the curve due to limitations of the range covered by certain of the circuit components. It can be seen from this curve that the units are not yet falling off at 6db per octave which suggests the possibility of the observed falloff being caused to some degree by the package design.

TABLE XI
COMPARISON OF COMMON BASE AND
COMMON EMITTER TUNED LINE AMPLIFIERS

Common Base Tuned Line Circuit - 500 mc

Unit No.	P_{in} Watts	V_{CB} Volts	I_C ma	PO Watts	PG db	η %
37-1	0.5	40	374	5.0	10	33.5
	1.0	40	295	5.8	7.64	49.0
	1.0	50	286	6.35	8.03	44.3

Common Emitter Tuned Line Circuit - 500 mc

Unit No.	P_{in} Watts	V_{CB} Volts	I_C ma	PO Watts	PG db	η %
37-1	1.0	40	195	3.1	4.92	39.7
	1.0	50	245	3.7	5.68	30.3

TABLE XII
HIGH FREQUENCY MEASUREMENTS OF EXPERIMENTAL
MODEL TA-2307 TRANSISTORS-COMMON EMITTER CONFIGURATION

Experimental Model Transistor Delivery Number 2

f = 50 Megacycles

Unit No.	P_{in} Watts	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
1	1.0	28	345	8.3	9.2	86
3	1.0	28	375	8.2	9.14	78
12	1.0	28	375	8.2	9.14	78
13	1.0	28	375	8.2	9.14	78
15	1.0	28	375	8.2	9.14	78
16	1.0	28	375	8.4	9.24	80
20	1.0	28	375	8.3	9.2	79

f = 150 Megacycles

1	1.0	28	165	3.2	5.06	69
3	1.0	28	195	3.4	5.32	62
12	1.0	28	175	3.4	5.32	69
13	1.0	28	205	3.5	5.44	61
15	1.0	28	205	3.3	5.19	57
16	1.0	28	140	3.0	4.77	77
20	1.0	28	205	3.5	5.44	61

Experimental Model Transistor Delivery Number 3

f = 400 Megacycles

25-2	0.5	50	170	3.4	8.32	40.0
26-2	0.5	50	130	3.4	8.32	52.3
26-4	0.5	50	150	3.6	8.57	48.0
26-5	0.5	50	140	3.8	8.8	54.3
26-10	0.5	50	160	3.6	8.57	45.0
26-11	0.5	50	150	3.9	8.92	52.0
25-2	1.0	50	175	4.7	6.72	53.7
26-2	1.0	50	180	4.7	6.72	52.2
25-4	1.0	50	200	5.1	7.08	51.0
26-5	1.0	50	180	4.8	6.82	53.3
26-10	1.0	50	160	4.4	6.43	55.0
26-11	1.0	50	200	5.0	6.99	50.0

TABLE XIII
COMPARISON OF COMMON EMITTER
LUMPED CONSTANT AND STUB TUNED AMPLIFIER CIRCUITS

400 Megacycle Lumped Constant Amplifier Circuit

Unit No.	P_{in} Watts	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
31-2	1.0	28	190	3.4	5.32	63.8
	1.0	50	190	5.4	7.32	56.9
31-3	1.0	28	200	3.1	4.92	55.4
	1.0	50	220	5.3	7.24	48.3

400 Megacycle Stub Tuned Amplifier Circuit

Unit No.	P_{in} Watts	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
31-2	1.0	28	190	3.6	5.56	67.6
	1.0	50	225	5.8	7.64	51.6
31-2	1.0	28	170	3.2	5.05	67.1
	1.0	50	205	5.4	7.32	52.7

TABLE XIV
500 MEGACYCLE POWER GAIN DATA ON FINAL TA-2507 TRANSISTORS

Final Delivery Number 1

Input Power = 0.5 Watt

Unit No.	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
37-27	50	295	3.7	8.68	25.0
34-13	50	308	3.4	8.30	22.1
37-7	50	235	3.0	7.77	25.5
37-9	50	295	2.7	7.32	18.3
37-23	50	240	2.2	6.42	18.6
30-20	50	164	2.25	6.52	27.2
34-42	50	240	2.3	6.62	19.1

Input Power = 1.0 Watt

37-27	50	360	5.2	7.16	28.9
34-13	50	270	5.0	7.0	37.0
41-34	50	330	4.7	6.72	28.5
34-19	50	275	4.6	6.63	33.9
37-30	50	305	4.6	6.63	30.2
37-33	50	355	4.5	6.53	25.3
34-18	50	275	4.5	6.53	32.7
37-5	50	285	4.4	6.43	30.9
37-7	50	285	4.4	6.43	30.9
41-33	50	335	4.4	6.43	26.3
37-9	50	282	4.2	6.23	29.9
41-32	50	420	4.2	6.23	20.0

TABLE XIV (Cont.)
500 MEGACYCLE POWER GAIN DATA ON FINAL TA-2307 TRANSISTORS

Input Power = 1.0 Watt

Unit No.	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
41-27	50	395	4.0	6.02	20.3
34-9	50	270	4.0	6.02	29.6
31-3	50	195	4.0	6.02	41.0
37-23	50	240	4.0	6.02	33.3
34-1	50	246	3.9	5.92	31.7
26-31	50	200	3.7	5.68	37.0
30-20	50	214	3.6	5.57	33.6
34-42	50	265	3.6	5.57	27.1

Final Delivery Number 2
Input Power = 1.0 Watt

37-20	50	312	5.0	7.0	32
37-22	50	365	3.9	5.9	21
37-25	50	360	5.2	7.15	29
37-28	50	344	5.0	7.0	29
37-29	50	280	5.4	7.4	38
40-11	40	356	4.0	6.0	28
40-14	40	320	3.5	5.4	27
40-21	40	320	4.0	6.0	31
40-28	40	378	3.5	5.4	23
41-1	40	310	3.6	5.56	29
41-2	40	310	4.0	6.02	32

TABLE XIV (Cont.)
500 MEGACYCLE POWER GAIN DATA ON FINAL TA-2307 TRANSISTORS

Input Power = 1.0 Watt

Unit No.	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
41-4	40	275	3.8	5.8	35
41-8	40	269	3.7	5.7	34
41-9	40	275	3.7	5.7	34
41-10	40	314	3.5	5.4	28
41-53	40	215	3.5	5.4	41
41-67	40	245	3.8	5.8	39
41-76	40	176	3.5	5.4	50
41-92	40	265	3.7	5.7	35
42-5	40	285	3.7	5.7	32
42-6	40	295	3.7	5.7	32
42-16	40	300	3.6	5.6	30
42-19	40	295	3.7	5.7	31
42-22	40	328	3.8	5.8	29
42-29	35	290	3.6	5.6	26
42-32	40	290	3.6	5.6	31
42-36	35	355	4.2	6.22	34
42-40	40	295	3.8	5.8	32
42-46	40	258	3.8	5.8	33
42-54	37	275	3.7	5.7	35
42-63	40	322	4.0	6.0	31
42-64	40	330	4.1	6.0	31

TABLE XIV(Cont.)
500 MEGACYCLE POWER GAIN DATA ON FINAL TA-2307 TRANSISTORS

Input Power = 1.0 Watt

Unit No.	V_{CE} Volts	I_C mA	PO Watts	PG db	η %
42-65	40	260	3.7	5.7	35
42-66	40	255	4.5	6.5	44
42-67	40	237	3.7	5.7	39
42-68	40	258	4.3	6.3	42
42-69	40	300	3.6	5.6	30
42-71	40	255	3.8	5.8	37
42-72	40	255	4.0	6.02	39
42-74	40	235	3.6	5.6	38
42-75	40	250	4.0	6.02	40
42-78	40	215	4.0	6.02	47
42-81	50	168	3.6	5.6	40
42-82	40	245	4.0	6.02	41
42-83	40	230	3.9	5.9	42
43-2	40	268	4.1	6.1	38
43-6	40	268	4.2	6.2	39
43-7	40	325	4.5	6.5	35
43-8	40	255	4.5	6.5	44
44-2	40	250	3.7	5.7	37
44-4	45	350	3.4	5.4	22
44-5	45	250	3.4	5.4	31
44-8	40	238	3.6	5.6	38

TABLE XIV (Cont.)
500 MEGACYCLE POWER GAIN DATA ON FINAL TA-2307 TRANSISTORS

Input Power = 1.0 Watt

Unit No.	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
44-12	40	275	4.5	6.5	41
44-21	40	275	4.2	6.2	38
44-26	40	230	3.6	5.6	39
44-27	40	240	3.6	5.6	37
44-33	40	380	4.0	6.0	26
44-36	40	258	3.7	5.7	36
44-38	40	246	3.6	5.6	36
44-41	40	280	3.8	5.8	34
44-43	40	265	3.7	5.7	35
44-46	50	236	4.0	6.0	34
44-52	40	295	3.7	5.7	31
44-53	40	287	4.2	6.2	36
44-54	40	242	3.8	5.8	39
44-56	40	285	4.7	6.7	41
44-57	40	275	4.5	6.5	41
44-58	40	275	4.2	6.2	38
44-63	40	285	4.0	6.0	36
44-65	40	255	3.6	5.6	35
44-66	40	295	3.8	5.8	32
44-70	40	265	4.1	6.1	39
44-71	40	260	3.6	5.6	34

TABLE XIV (Cont.)
500 MEGACYCLE POWER GAIN DATA ON FINAL TA-2307 TRANSISTORS

Input Power = 1.0 Watts

Unit No.	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
44-72	40	267	4.1	6.1	38
44-73	40	238	3.7	5.7	39
44-76	40	245	4.0	6.0	41
44-78	40	245	4.0	6.0	41
44-79	50	300	4.9	6.9	33
44-80	40	225	4.0	6.0	45
44-81	40	228	3.9	5.9	43
44-82	40	213	3.7	5.7	37
44-84	40	250	3.9	5.9	40
44-85	40	233	3.8	5.8	40
44-86	40	220	4.2	6.2	33
44-87A	40	207	3.5	5.5	42
44-87	40	190	3.5	5.5	46
44-93	40	268	4.2	6.2	39
44-94	40	275	4.5	6.5	41
44-95	40	230	3.8	5.8	41
44-96	40	230	4.1	6.1	44
44-97	40	243	3.5	5.5	36
44-98	40	295	4.5	6.5	38
44-100	40	246	4.6	6.0	40
44-104	40	304	4.6	6.6	38

TABLE XIV (Cont.)
500 MEGACYCLE POWER GAIN DATA ON FINAL TA-2307 TRANSISTORS

Input Power = 1.0 Watts

Unit No.	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
44-105	40	225	3.4	5.4	39
44-108	40	250	3.9	5.9	39
44-109	40	270	3.9	5.9	37
44-110	40	235	3.9	5.9	42
44-104	40	303	4.5	6.5	37
44-113	40	285	3.6	5.6	32
44-114	40	305	4.2	6.2	34
44-116	40	268	3.6	5.6	34
44-118	40	198	3.5	5.5	44
44-121	40	246	3.8	5.8	38
44-123	40	195	3.6	5.6	34
44-124	50	278	4.5	6.5	24
44-127	40	245	3.9	5.9	40
44-131	40	248	3.95	5.9	40
44-134	40	225	3.6	5.6	40
44-136	40	265	3.9	5.9	37
44-137	40	235	3.6	5.6	39
44-138	40	230	3.6	5.6	39
44-139	50	228	4.0	6.0	35
44-140	40	256	3.7	5.7	36
44-141	40	246	3.9	5.9	39

TABLE XIV (Cont.)
500 MEGACYCLE POWER GAIN DATA ON FINAL TA-2307 TRANSISTORS

Input Power = 1.0 Watts

Unit No.	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
44-147	40	272	3.8	5.8	34
44-148	40	205	4.2	6.2	51
44-151	40	233	3.9	5.9	42
44-152	40	243	3.6	5.6	37
44-154	40	315	4.2	6.2	33
44-159	40	260	4.1	6.1	39
44-160	40	340	4.8	6.8	35
44-167	40	305	4.1	6.1	33
44-168	40	300	3.9	5.9	32
44-169	40	270	4.2	6.2	39
44-170	40	238	3.6	5.6	38
44-171	40	285	4.3	6.3	38
44-172	40	292	4.2	6.2	36
44-174	40	315	4.6	6.6	36
44-175	40	256	3.9	5.9	38
44-180	40	250	3.9	5.9	39
44-181	40	278	3.7	5.7	34
44-182	40	265	3.5	5.5	33
44-183	40	312	4.6	6.6	37
44-184	40	255	3.7	5.7	34
44-186	40	260	3.7	5.7	35

TABLE XIV (Cont.)
500 MEGACYCLE POWER GAIN DATA ON FINAL TA-2307 TRANSISTORS

Input Power = 1.0 Watts

Unit No.	V_{CE} Volts	I_C ma	PO Watts	PG db	η %
44-187	40	292	4.2	6.2	36
44-190	40	315	4.5	6.5	36
44-193	40	295	4.0	6.0	34
44-196	40	260	4.0	6.0	39
44-199	40	240	3.5	5.4	37
44-202	40	275	3.5	5.4	38
44-204	40	230	3.5	5.4	37
44-206	40	245	3.6	5.6	41
44-209	40	230	3.8	5.8	34
44-211	40	260	4.1	6.1	39
44-213	40	238	4.0	6.0	42
44-214	40	290	4.1	6.1	35
44-215	40	255	3.5	5.4	37
44-218	40	240	3.6	5.6	42
44-219	40	220	3.7	5.7	39
44-225	40	258	3.7	5.7	38
44-230	40	256	3.9	5.9	36
44-231	40	256	4.1	6.1	40
44-232	40	265	3.8	5.8	41
44-252	40	212	3.5	5.4	43
45-1	40	220	3.6	5.6	44

TABLE XIV (Cont.)
500 MEGACYCLE POWER GAIN DATA ON FINAL TA-2307 TRANSISTORS

Input Power = 1.0 Watts

Unit No.	V_{CE} Volts	I_C ma.	PO Watts	PG db	η %
45-2	40	200	3.6	5.6	45
45-3	40	223	4.0	6.0	45
45-6	40	220	4.2	6.2	47
45-8	40	234	4.0	6.0	43
45-9	40	265	4.0	6.0	38
45-10	40	247	4.3	6.3	44
45-12	40	230	4.1	6.1	45
45-13	40	250	4.0	6.0	40
45-14	40	200	3.9	5.9	49
45-17	50	275	4.6	6.6	38
45-20	40	234	3.6	5.6	39
45-21	40	262	4.3	6.3	41
45-22	40	190	3.8	5.8	50
45-23	40	287	5.0	7.0	34
45-26	40	204	3.8	5.8	46
45-29	40	213	3.6	5.6	42
45-30	40	194	3.5	5.5	45
45-34	40	268	4.1	6.1	38
45-35	40	245	3.8	5.8	39
45-36	40	223	4.3	6.3	48
45-39	40	235	4.1	6.1	48
45-41	40	222	4.2	6.2	44

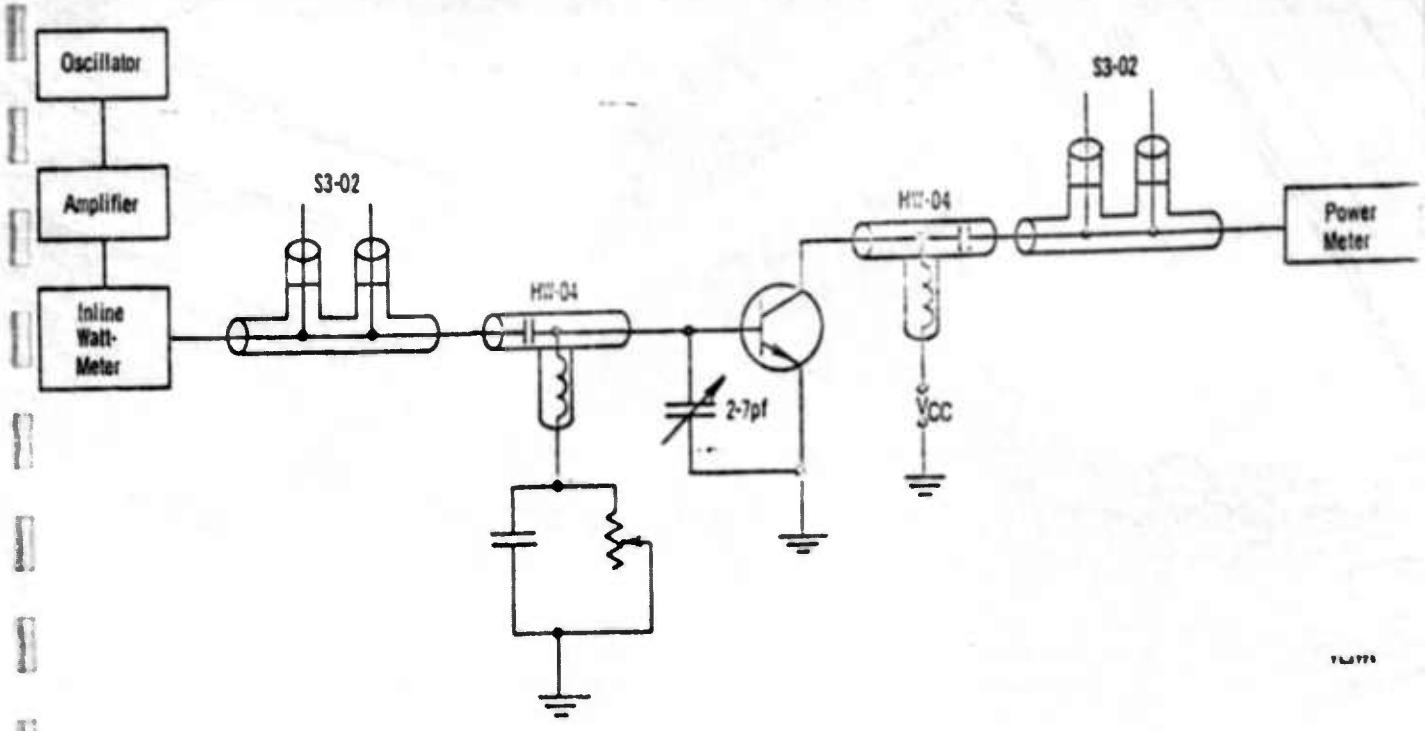


FIGURE 36 CLASS C COMMON EMITTER TUNED LINE AMPLIFIER CIRCUIT

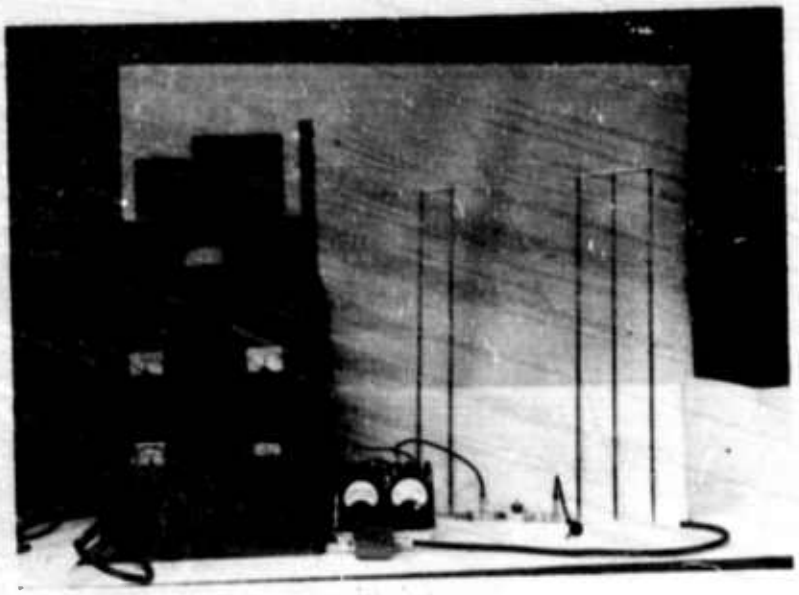


FIGURE 37 500 MEGACYCLE POWER GAIN TEST SET

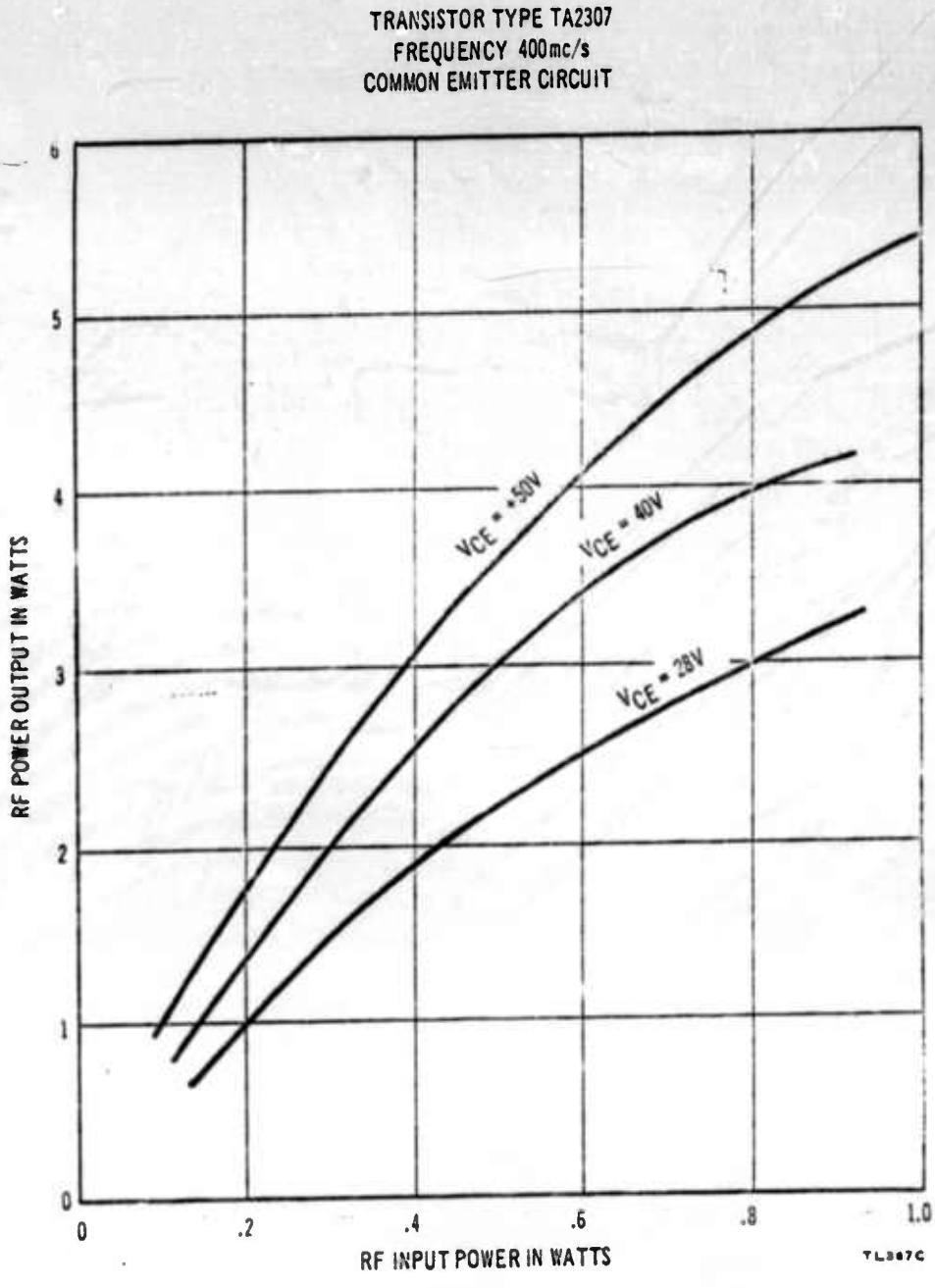


FIGURE 38 RF OUTPUT POWER VERSUS RF INPUT POWER AT VARIOUS COLLECTOR SUPPLY VOLTAGES

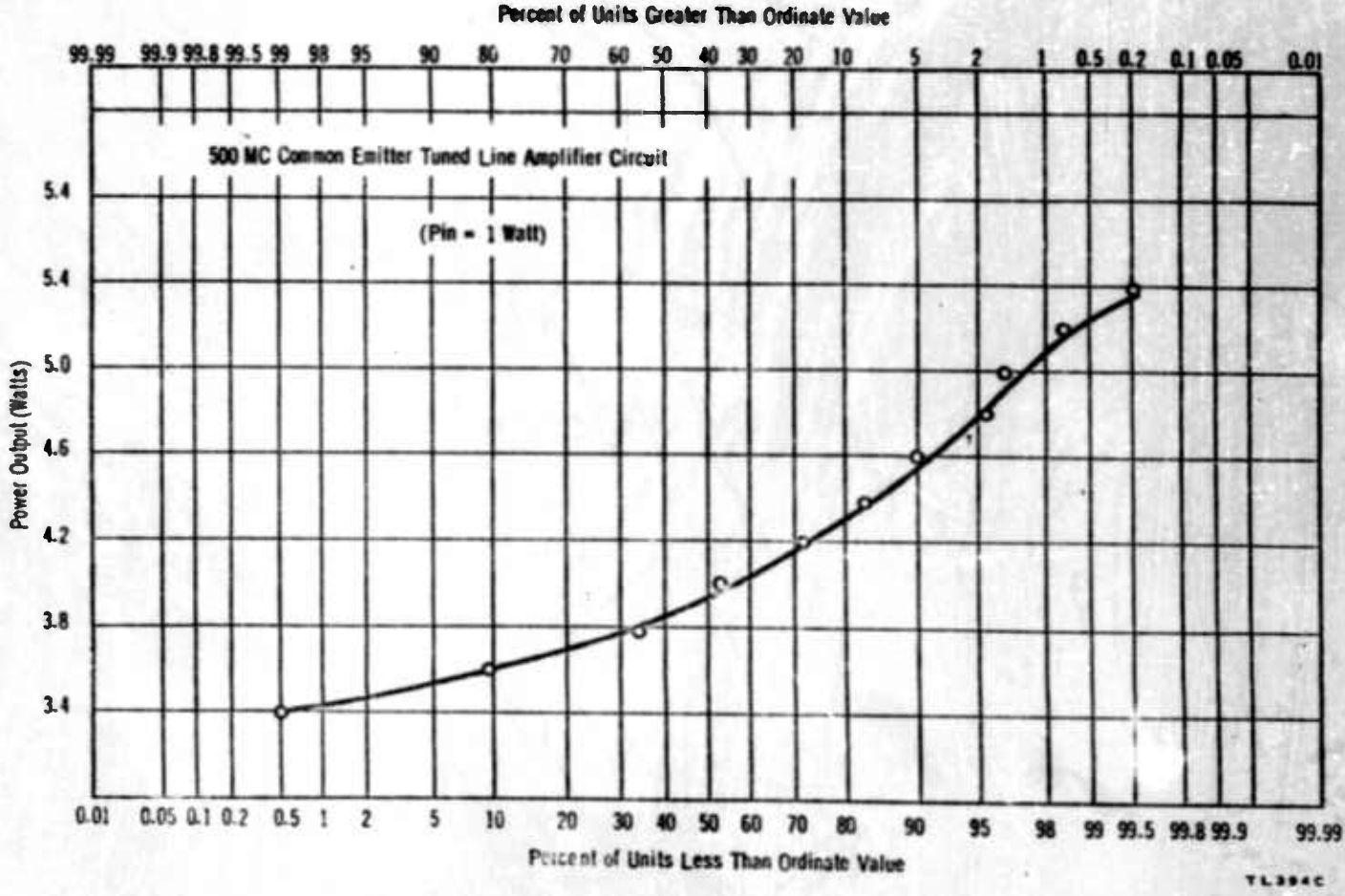


FIGURE 39 DISTRIBUTION OF POWER OUTPUT ON TA2307 FINAL TRANSISTORS

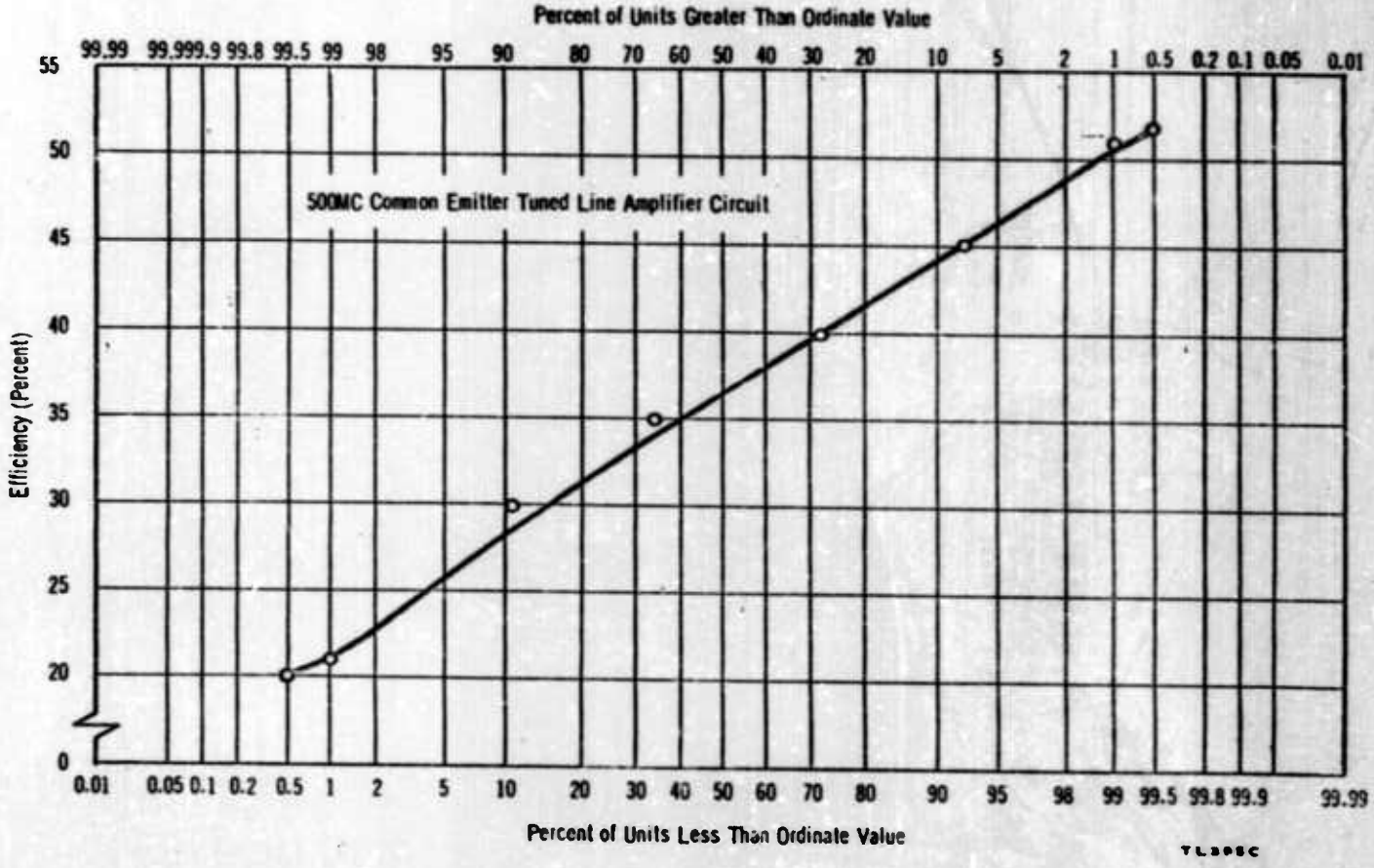


FIGURE 40 DISTRIBUTION OF CIRCUIT EFFICIENCY ON TA2307 FINAL TRANSISTORS

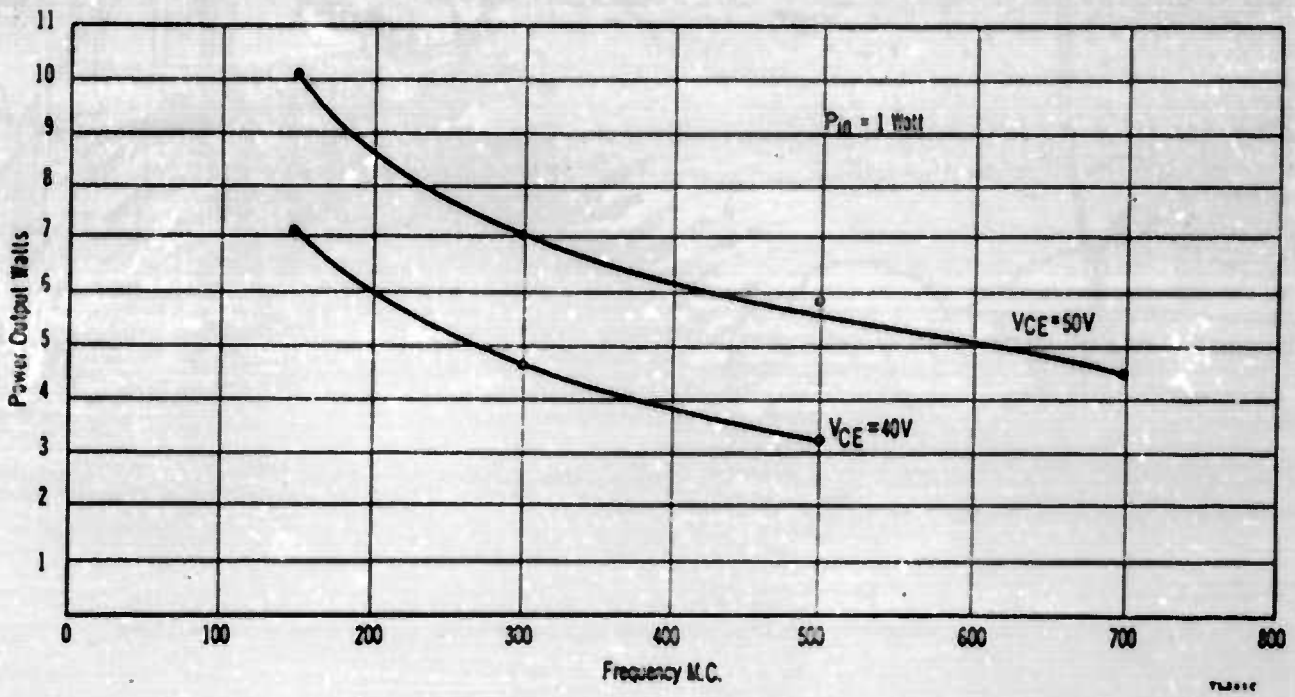


FIGURE 41 POWER OUTPUT VERSUS FREQUENCY

V. OVERALL CONCLUSIONS

A unique transistor geometry, called the overlay structure, was designed which affords considerable advantages over the interdigitated (comb) structure. This geometry results in high design ratios of emitter periphery to emitter area and emitter periphery to base area which have an important influence on the gain-bandwidth product of transistors.

These improved design ratios are, to a large extent, the result of the emitter diffusion pattern. This pattern uses many small squares arranged in an array instead of the few narrow stripes associated with comb type devices.

The feasibility of the originally proposed approach, using the anodic formation of Al_2O_3 over the base metallizing matrix, has been shown by the fabrication of several devices exhibiting amplifier performance at low current levels. It was felt, however, that the fabrication problems associated with this approach were too numerous to be solved within the contract period.

State-of-the-art advances in the techniques of photomask fabrication, photolithography and diffusion during development of this device were employed in the design and development of a diffused overlay structure. This structure retained the advantages of the originally proposed device but greatly reduced the fabrication difficulties.

Common emitter, Class C, 500 megacycle tuned line amplifiers were designed and constructed for ultrahigh frequency measurements of the final devices.

Two hundred final transistors fabricated in the modified structure delivered 500 megacycle output powers of 3.4 to 5.4 watts with one watt of input drive. The median of these units delivered 4.0 watts with 6db of gain.

The progress realized during this contract period has resulted in the fabrication of silicon transistors capable of high power, ultrahigh frequency operation far beyond the previous state-of-the-art devices. The advances attained in semiconductor technology allow the development of future devices that require extremely small geometries and very shallow diffusions and further extends the operating frequency range of silicon transistors.

VI. RECOMMENDATIONS

The importance of the base width and intrinsic material width for ultrahigh frequency operation has been discussed. To take full advantage of the breakdown voltage available for particular base and intrinsic material widths, a thorough investigation of surface effects is recommended. Further studies on the use of highly doped layers as conductors are also essential for additional improvement of the overlay structure.

Studies of ultrahigh frequency case designs are required which will allow transistors to be packaged in cases giving the least degradation of performance.

VII. PERSONNEL AND MAN HOURS

THIS SECTION WILL BE COMPLETED UPON APPROVAL OF THE DRAFT COPY.

VIII. REFERENCES

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